Geïntegreerde proef 6de jaar Industriële Wetenschappen

RADAR

Principe en werking

Bijlagen

VTI Torhout
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1999-2000

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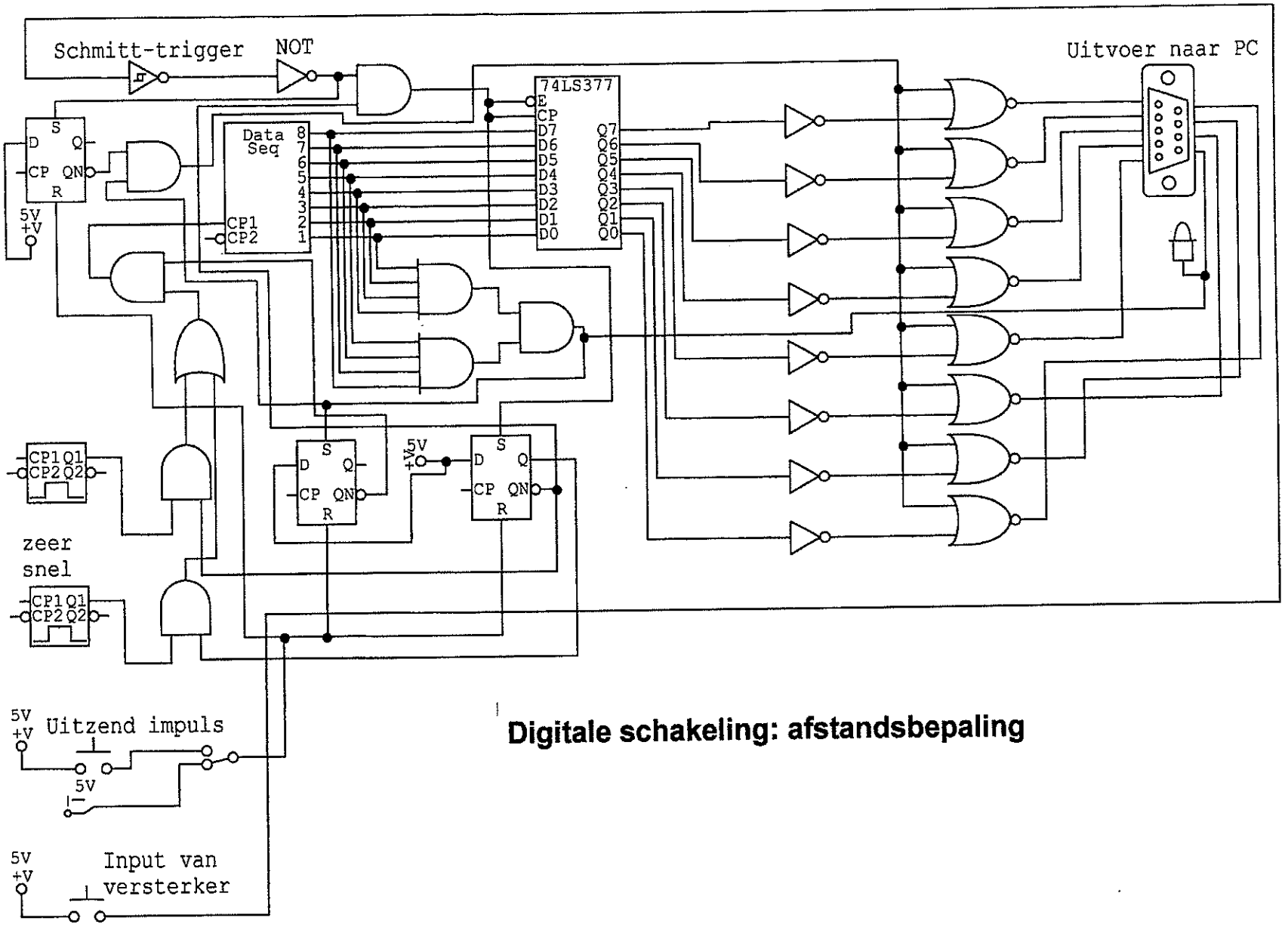
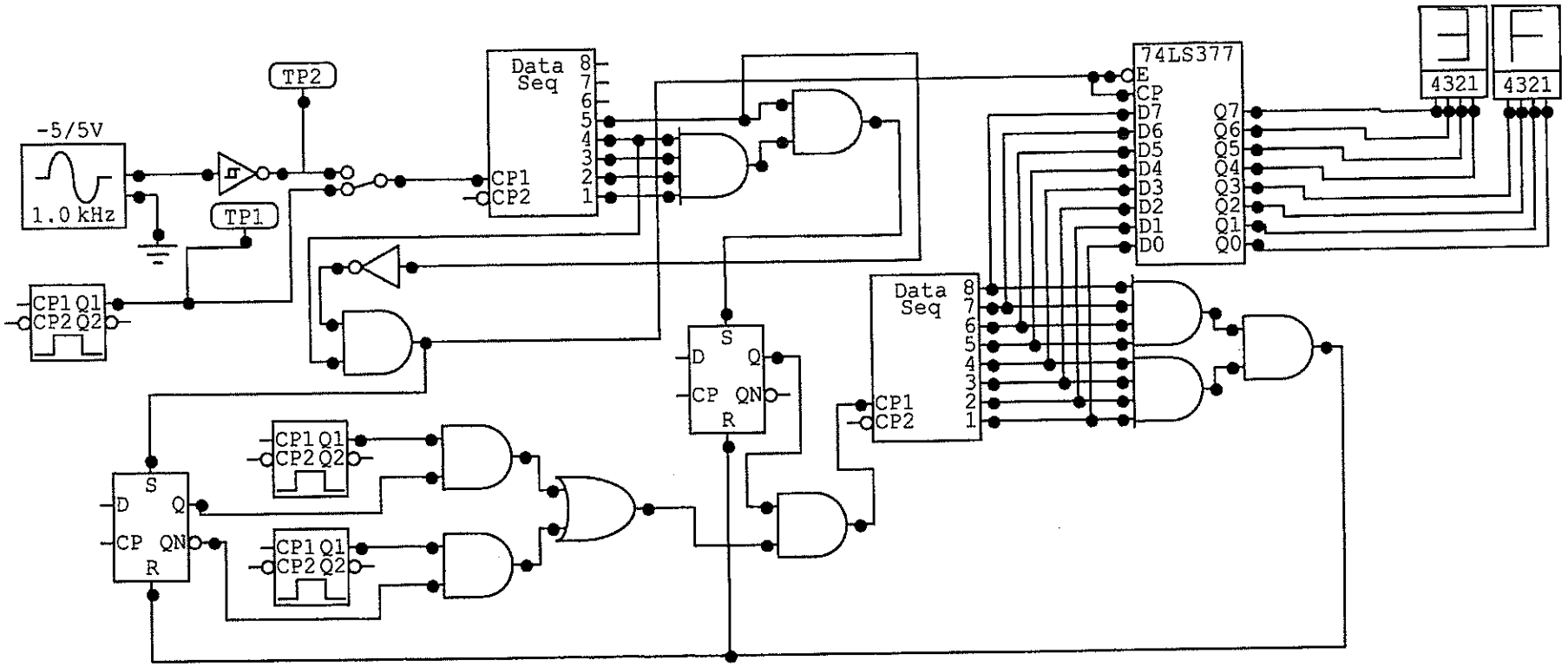
Jonas Missiaen
Gerd Vermont

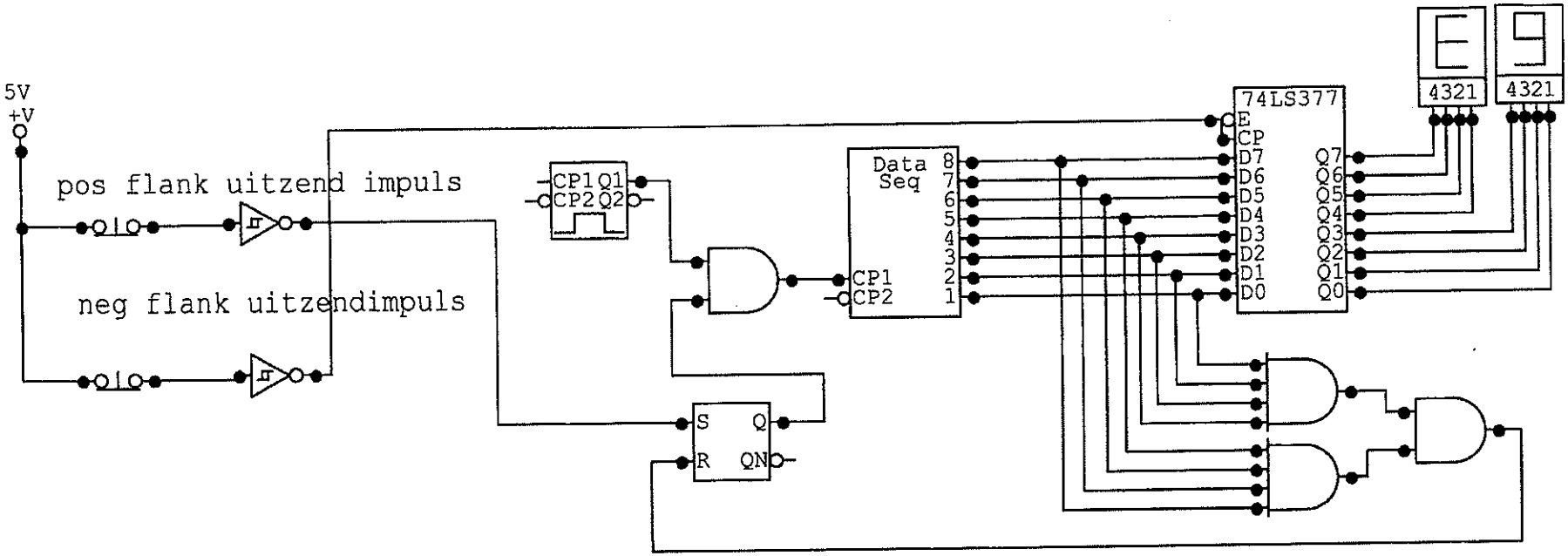
Bijlagen



Digitale schakeling: afstandsbepaling



Digitale schakeling: Snelheidsbepaling voor radar die constant uitzendt



Digitale schakeling: Snelheidsbepaling voor radar die pulsen uitzendt

SILICON PLANAR EPITAXIAL TRANSISTORS

General purpose n-p-n transistors in a plastic TO-92 variant, especially suitable for use in driver stages of audio amplifiers.

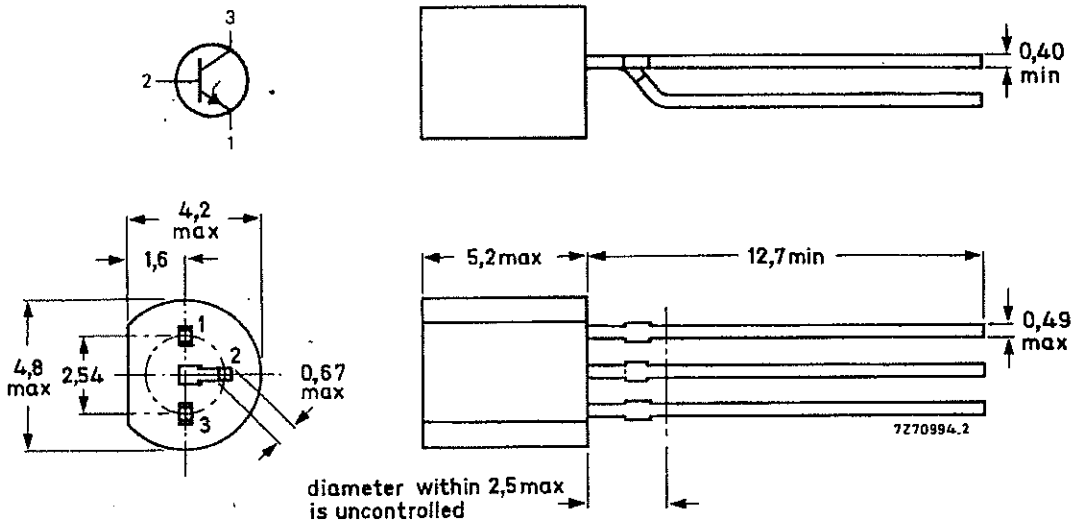
QUICK REFERENCE DATA

			BC546	BC547	BC548	
Collector-emitter voltage (V_{BE} = 0)	V_{CES}	max.	80	50	30	V
Collector-emitter voltage (open base)	V_{CEO}	max.	65	45	30	V
Collector current (peak value)	I_{CM}	max.	200	200	200	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	500	500	500	mW
Junction temperature	T_j	max.	150	150	150	°C
D.C. current gain I_C = 2 mA; V_{CE} = 5 V	h_{FE}	>	110	110	110	
		<	450	800	800	
Transition frequency I_C = 10 mA; V_{CE} = 5 V	f_T	typ.	300	300	300	MHz
Noise figure at R_S = 2 kΩ I_C = 200 μA; V_{CE} = 5 V f = 1 kHz; B = 200 Hz	F	typ.	2	2	2	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BC546	BC547	BC548	
Collector-base voltage (open emitter)	V_{CBO}	max.	80	50	30	V
Collector-emitter voltage ($V_{BE} = 0$)	V_{CES}	max.	80	50	30	V
Collector-emitter voltage (open base)	V_{CEO}	max.	65	45	30	V
Emitter-base voltage (open collector)	V_{EBO}	max.	6	6	5	V
Collector current (d.c.)	I_C			max.	100	mA
Collector current (peak value)	I_{CM}			max.	200	mA
Emitter current (peak value)	$-I_{EM}$			max.	200	mA
Base current (peak value)	I_{BM}			max.	200	mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}			max.	500	mW
Storage temperature	T_{stg}			−65 to + 150		^oC
Junction temperature	T_j			max.	150	^oC

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	0,25	K/mW
From junction to case	$R_{th\ j\text{-}c}$	=	0,15	K/mW

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

Collector cut-off current				
$I_E = 0$; $V_{CB} = 30$ V	I_{CBO}	<	15	nA
$I_E = 0$; $V_{CB} = 30$ V; $T_j = 150\ ^oC$	I_{CBO}	<	5	μA
Base-emitter voltage*				
$I_C = 2$ mA; $V_{CE} = 5$ V	V_{BE}	typ.	660	mV
			580 to 700	mV
$I_C = 10$ mA; $V_{CE} = 5$ V	V_{BE}	<	770	mV

Saturation voltage*					
I_C = 10 mA; I_B = 0,5 mA	V_{CEsat}		typ.	90	mV
			<	250	mV
	V_{BEsat}		typ.	700	mV
I_C = 100 mA; I_B = 5 mA	V_{CEsat}		typ.	200	mV
			<	600	mV
	V_{BEsat}		typ.	900	mV
Collector capacitance at f = 1 MHz $I_E = I_e$ = 0; V_{CB} = 10 V	C_c		typ.	2,5	pF
Emitter capacitance at f = 1 MHz $I_C = I_c$ = 0; V_{EB} = 0,5 V	C_e		typ.	9	pF
Transition frequency at f = 35 MHz I_C = 10 mA; V_{CE} = 5 V	f_T		typ.	300	MHz
Small signal current gain at f = 1 kHz I_C = 2 mA; V_{CE} = 5 V	h_{fe}		125 to 900		

			BC546	BC547	BC548
Noise figure at R_S = 2 kΩ I_C = 200 μA; V_{CE} = 5 V f = 1 kHz; B = 200 Hz	F	typ.	2	2	2 dB
		<	10	10	10 dB

			BC546A BC547A BC548A	BC546B BC547B BC548B	BC547C BC548C
D.C. current gain I_C = 10 μA; V_{CE} = 5 V	h_{FE}	typ.	90	150	270
		>	110	200	420
I_C = 2 mA; V_{CE} = 5 V	h_{FE}	typ.	180	290	520
		<	220	450	800

* V_{BEsat} decreases by about 1,7 mV/K with increasing temperature.

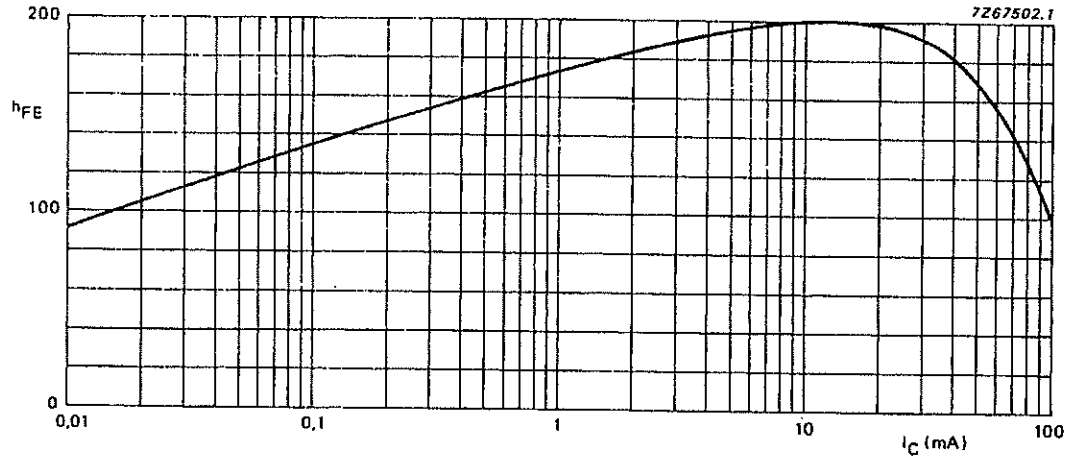


Fig. 2 BC546A, BC547A and BC548A
V_{CE} = 5 V; T_j = 25 °C; typical values.

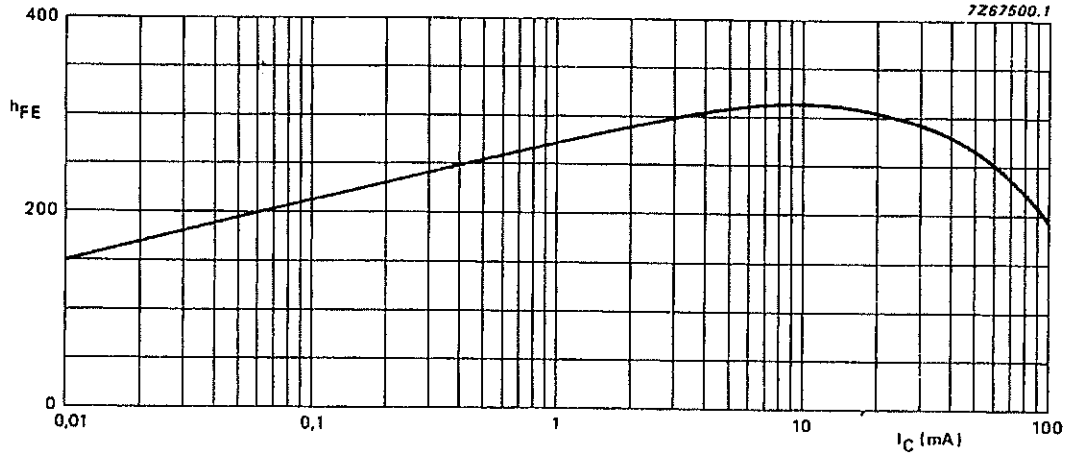


Fig. 3 BC546B, BC547B and BC548B
V_{CE} = 5 V; T_j = 25 °C; typical values.

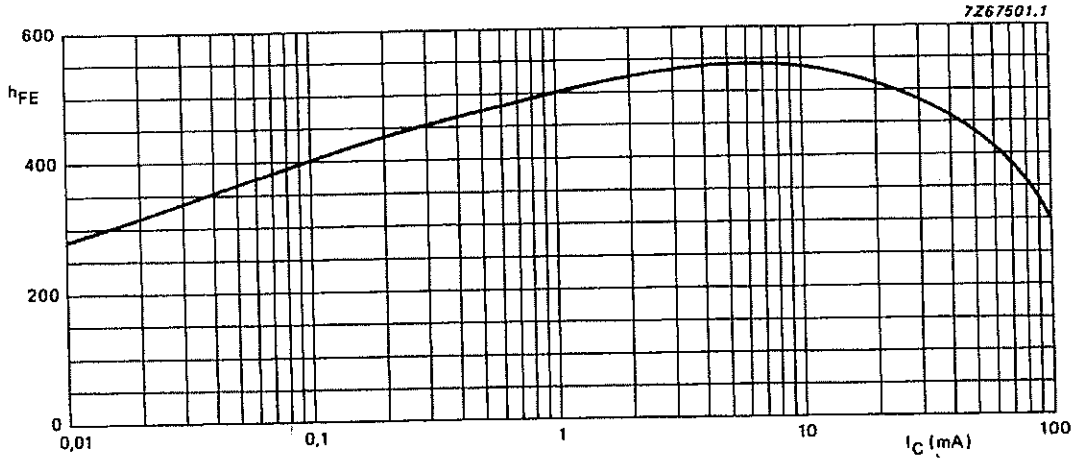


Fig. 4 BC547C and BC548C
V_{CE} = 5 V; T_j = 25 °C; typical values.

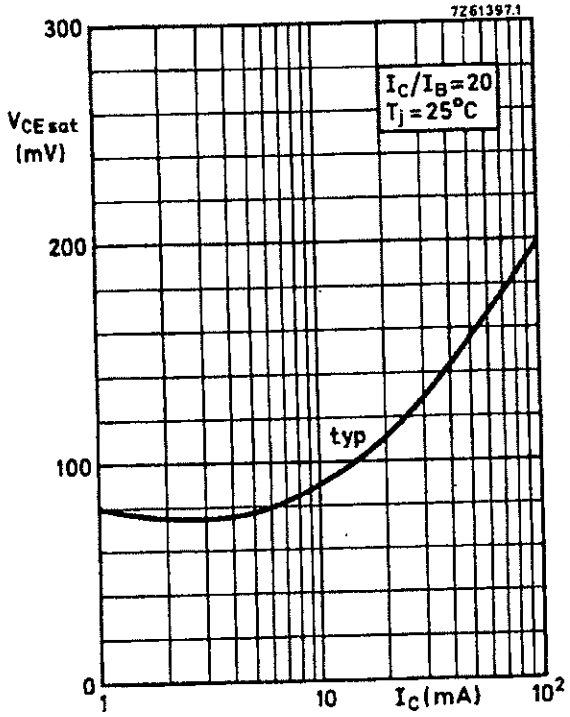


Fig. 5.

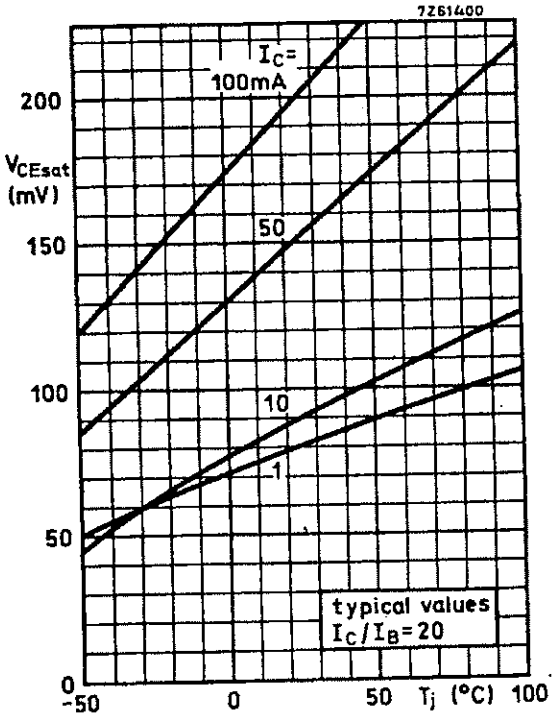


Fig. 6.

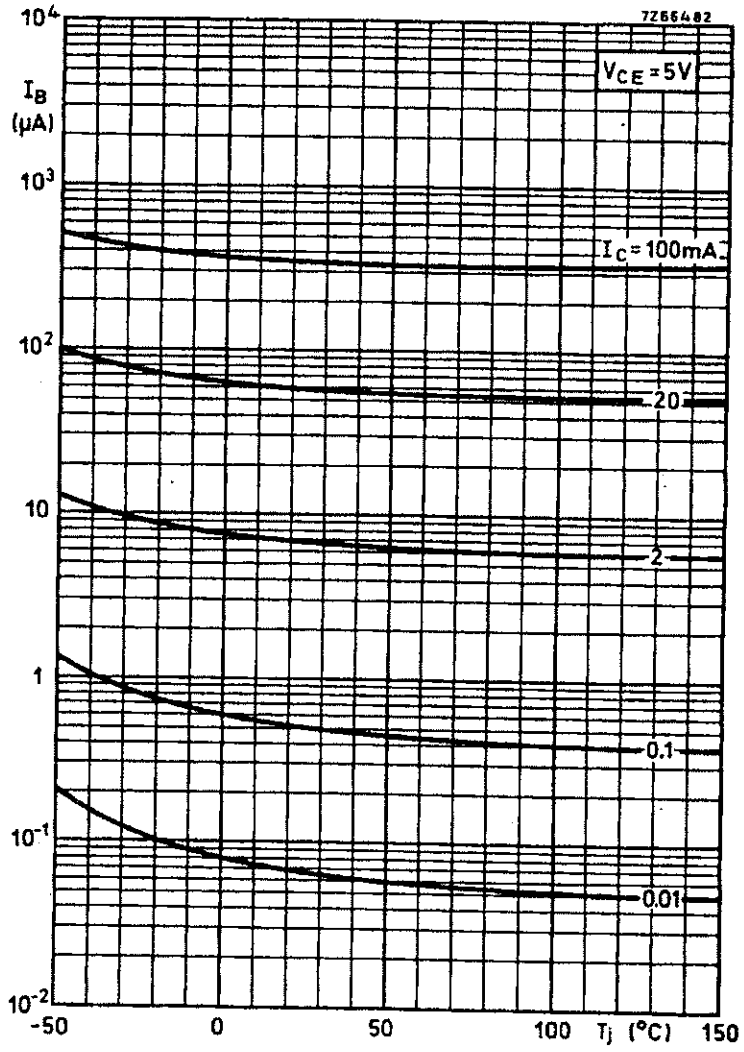

7Z66482
10^4
I_B
(μA)
10^3
10^2
10
1
10^{-1}
10^{-2}
V_{CE} = 5V
I_C = 100mA
20
2
0.1
0.01
-50
0
50
100
T_j (°C)
150

Fig. 7.

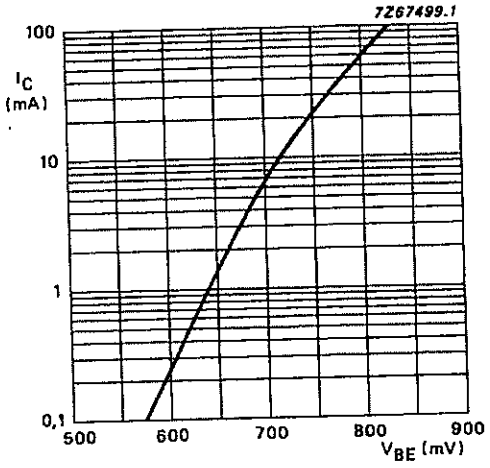


Fig. 8 V_{CE} = 5 V; T_j = 25 °C; typical values.

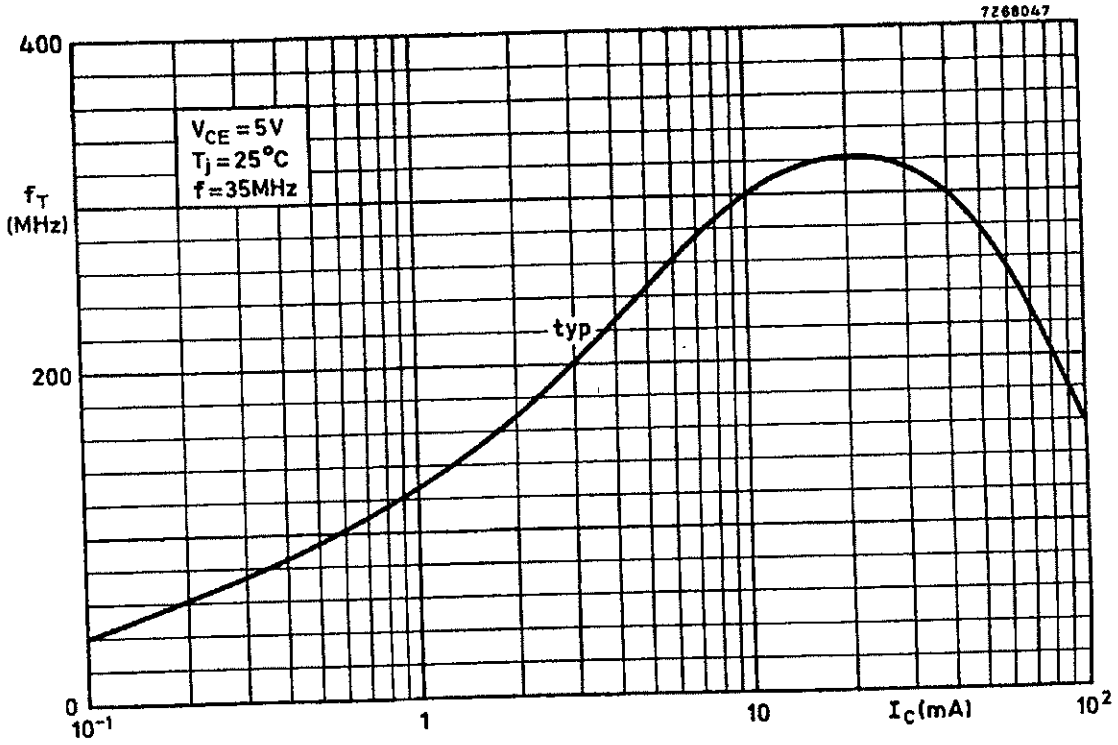


Fig. 9.

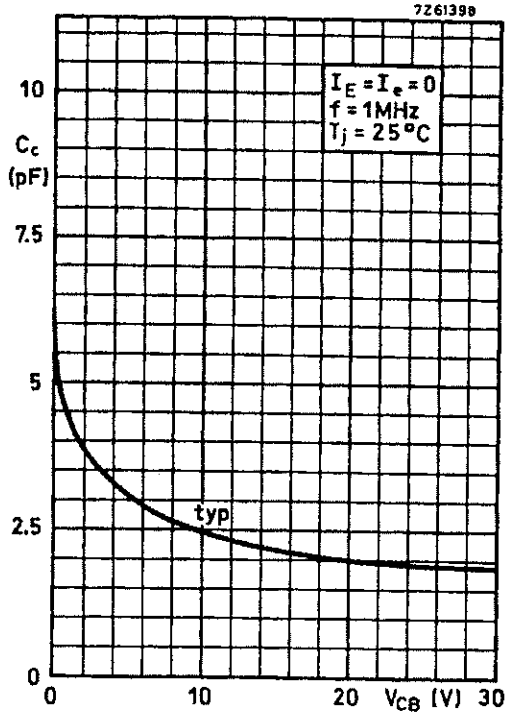
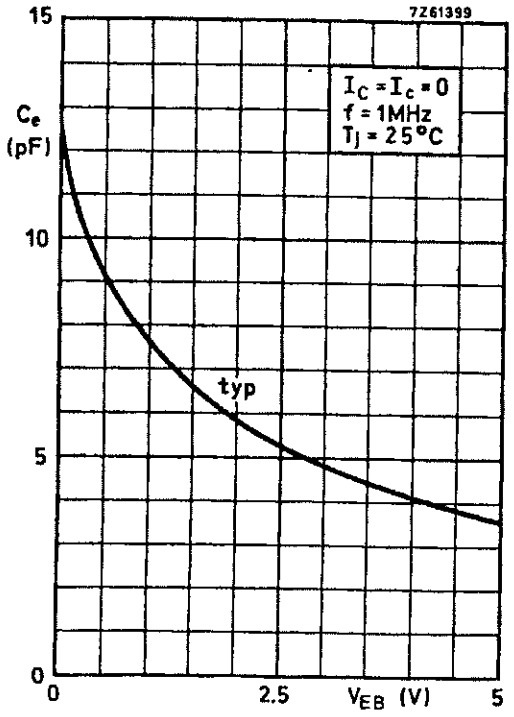

7Z61398
$I_E = I_e = 0$
f = 1MHz
T_j = 25°C
C_c (pF)
10
7.5
5
2.5
0
typ
0
10
20
V_{CB} (V)
30

Fig. 10.


7Z61399
$I_C = I_c = 0$
f = 1MHz
T_j = 25°C
C_e (pF)
15
10
5
0
typ
0
2.5
V_{EB} (V)
5

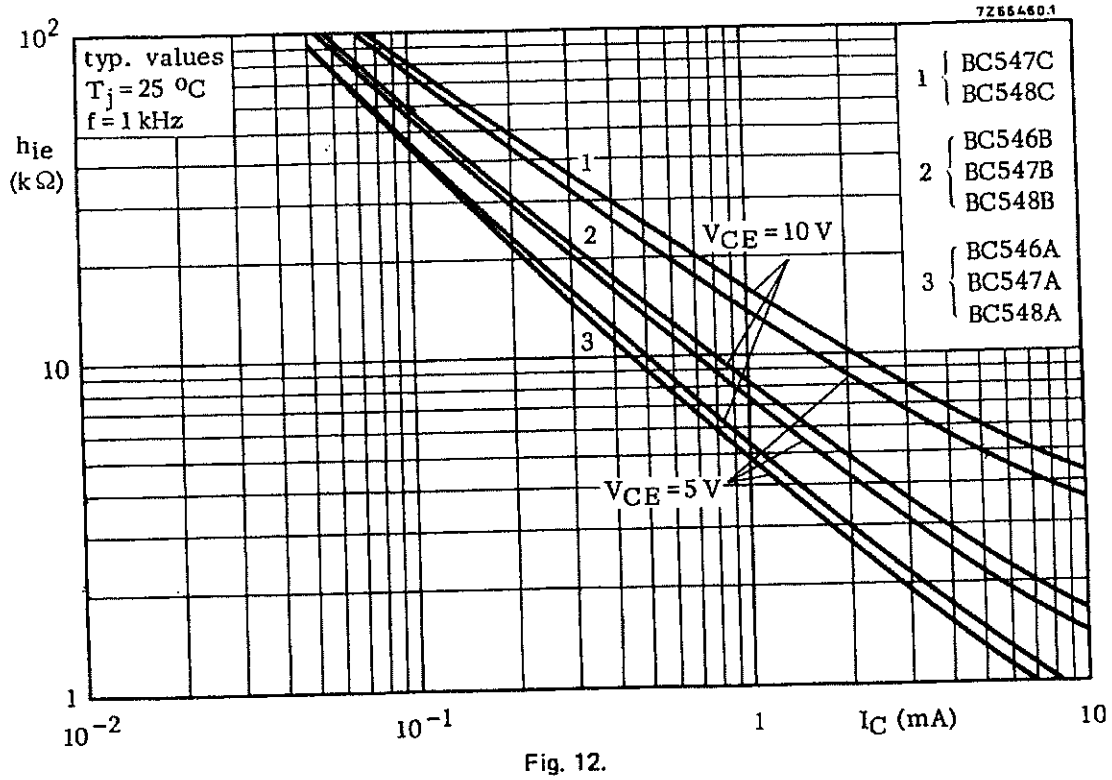

7Z66460.1
typ. values
T_j = 25 °C
f = 1 kHz
h_{ie} (kΩ)
10^2
10
1
10^{-2}
10^{-1}
1
10
I_C (mA)
1 { BC547C BC548C
2 { BC546B BC547B BC548B
3 { BC546A BC547A BC548A
V_{CE} = 10 V
V_{CE} = 5 V

Fig. 12.

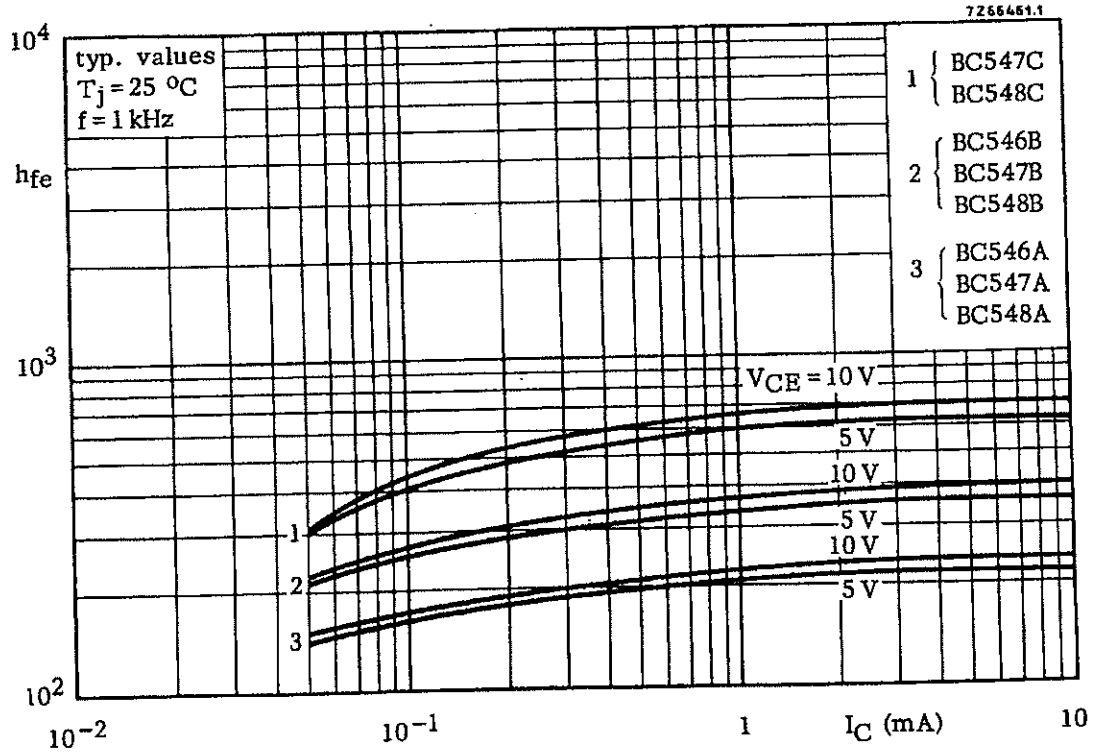

7Z66461.1
typ. values
T_j = 25 °C
f = 1 kHz
h_{fe}
10^4
10^3
10^2
10^{-2}
10^{-1}
1
10
I_C (mA)
1 { BC547C BC548C
2 { BC546B BC547B BC548B
3 { BC546A BC547A BC548A
V_{CE} = 10 V
5 V
10 V
5 V
10 V
5 V

Fig. 13

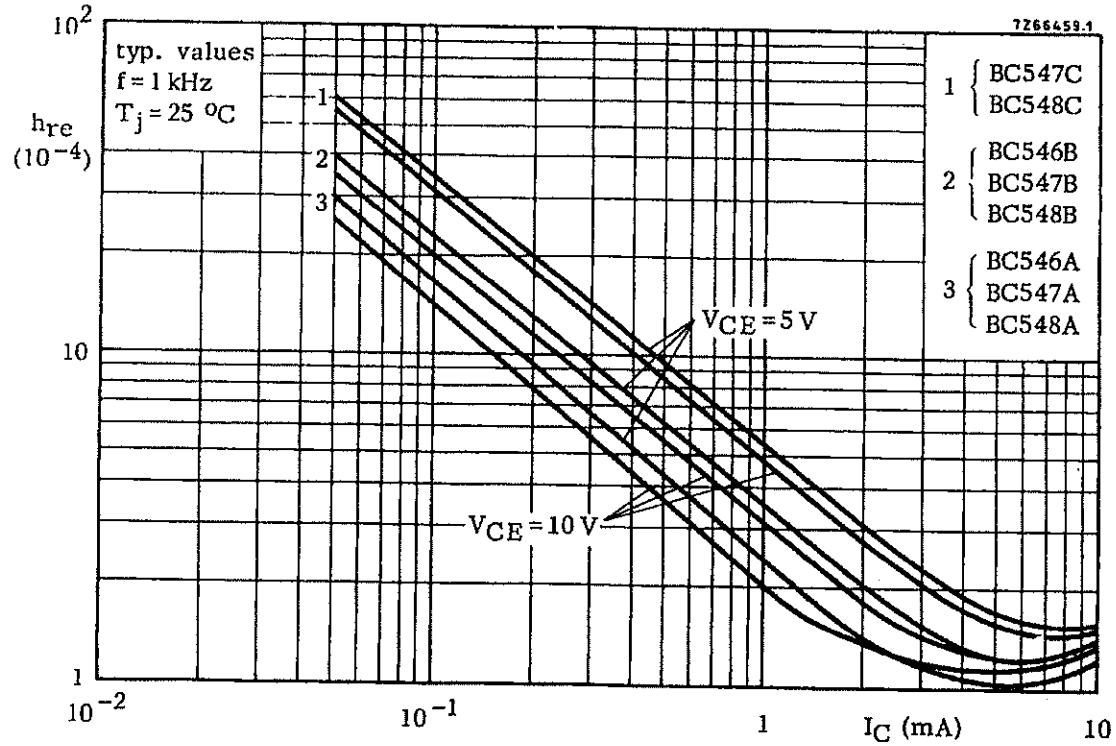

7Z66459.1
typ. values
f = 1 kHz
T_j = 25 °C
h_{re} (10^{-4})
10^2
10
1
10^{-2}
10^{-1}
1
10
I_C (mA)
1 { BC547C BC548C
2 { BC546B BC547B BC548B
3 { BC546A BC547A BC548A
V_{CE} = 5 V
V_{CE} = 10 V

Fig. 14.

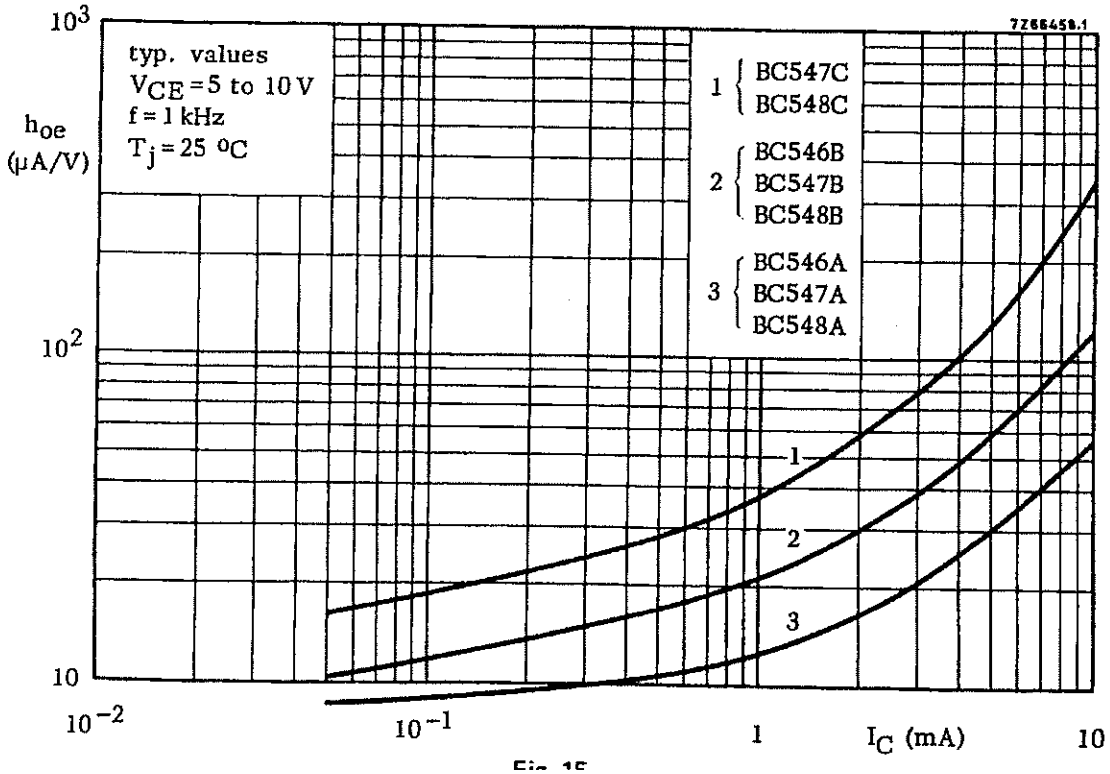

7Z66458.1
typ. values
V_{CE} = 5 to 10 V
f = 1 kHz
T_j = 25 °C
h_{oe} (μA/V)
10^3
10^2
10
10^{-2}
10^{-1}
1
10
I_C (mA)
1 { BC547C BC548C
2 { BC546B BC547B BC548B
3 { BC546A BC547A BC548A

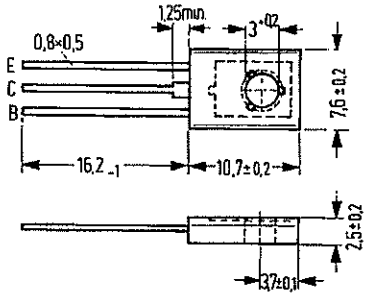
Fig. 15.

für NF-Treiber- und Endstufen mittlerer Leistung

BD 135, BD 137 und BD 139 sind epitaktische NPN-Silizium-Planar-Transistoren in Kunststoffgehäuse 12 A 3 DIN 41869 Bl. 4 (TO-126). Der Kollektor ist mit der metallischen Montagefläche des Transistors leitend verbunden. Die Transistoren sind besonders in Verbindung mit BD 136, BD 138 und BD 140 als komplementäre Transistorpaare für Treiberstufen in NF-Verstärkern mit hohen Ausgangsleistungen verwendbar.

Typ	Bestellnummer
BD 135	Q62702-D106
BD 135-6	Q62702-D106-V1
BD 135-10	Q62702-D106-V2
BD 135-16	Q62702-D106-V3
BD 135 gep.	Q62702-D106-P
BD 137	Q62702-D108
BD 137-6	Q62702-D108-V1
BD 137-10	Q62702-D108-V2
BD 137 gep.	Q62702-D108-P
BD 139	Q62702-D110
BD 139-6	Q62702-D110-V1
BD 139-10	Q62702-D110-V2
BD 139 gep.	Q62702-D110-P
BD 135/BD 136 kompl. gep.	Q62702-D139-S1
BD 137/BD 138 kompl. gep.	Q62702-D140-S1
BD 139/BD 140 kompl. gep.	Q62702-D141-S1

Typ	Bestellnummer
Glimmerscheibe	Q62902-B62
Federscheibe A 3 DIN 137	Q62902-B63



Gewicht etwa 0,5 g — Maße in mm

Transistor-Befestigung mit M3-Schraube, Anzugsmoment < 0,8 Nm. (Unterlagscheibe oder Federscheibe verwenden!)

[1]) Der Wärmewiderstand erhöht sich mit der 50 µ starken Glimmerscheibe (ungefettet) um 8 K/W; und gefettet um 4 K/W.

Grenzdaten		BD 135	BD 137	BD 139	
Kollektor-Emitter-Spannung ($R_{BE} \leqq 1$ kΩ)	U_{CER}	–	–	100	V
Kollektor-Basis-Spannung	U_{CBO}	45	60	–	V
Kollektor-Emitter-Spannung	U_{CEO}	45	60	80	V
Emitter-Basis-Spannung	U_{EBO}	5	5	5	V
Kollektor-Spitzenstrom	I_{CM}	2,0	2,0	2,0	A
Kollektorstrom	I_C	1,5	1,5	1,5	
Basisstrom	I_B	0,2	0,2	0,2	A
Sperrschichttemperatur	T_j	150	150	150	°C
Lagertemperatur	T_s		−55 bis +125		°C
Gesamtverlustleistung ($T_G \leqq 25$ °C)	P_{tot}	12,5	12,5	12,5	W
Wärmewiderstand					
Kollektorsperrschicht – Luft	R_{thJU}	≦ 110	≦ 110	≦ 110	K/W
Kollektorsperrschicht – Transistorgehäuseboden	R_{thJG}[1])	≦ 10	≦ 10	≦ 10	K/W

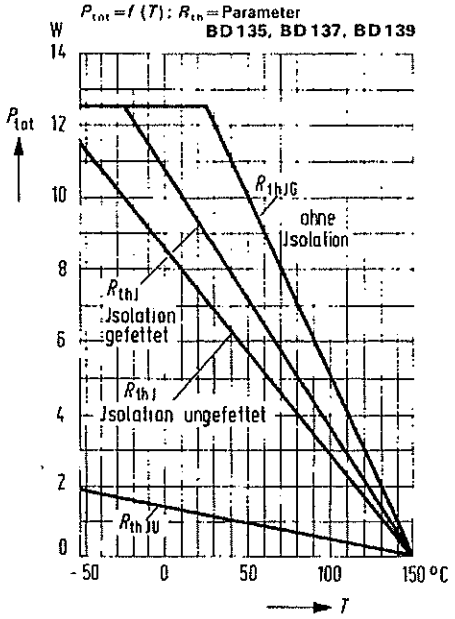
Statische Kenndaten ($T_U = 25°C$)

Die Transistoren BD 135, BD 137 und BD 139 werden bei $U_{CE} = 2$ V nach der statischen Stromverstärkung B gruppiert und mit Zahlen der DIN-Normenreihe gekennzeichnet.

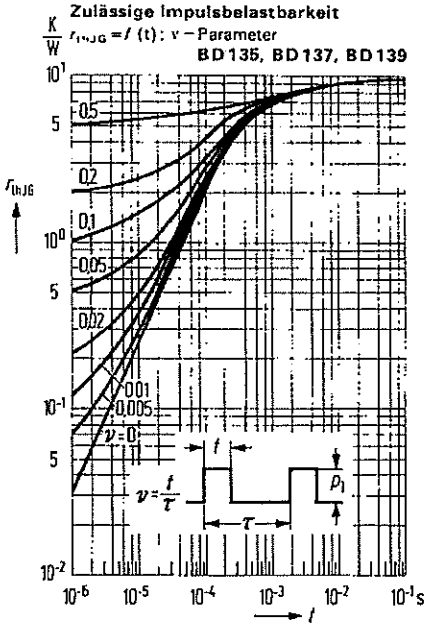
B-Gruppe	6	10	16	
Typ	**BD 135** **BD 137** **BD 139**	**BD 135** **BD 137** **BD 139**	**BD 135** – –	**BD 135** **BD 137** **BD 139**
I_C (mA)	B I_C/I_B	B I_C/I_B	B I_C/I_B	U_{BE} (V)
5	> 25	> 25	> 25	–
150	63 (40 bis 100)	100 (63 bis 160)	160 (100 bis 250)	–
500	> 25	> 25	> 25	1,2

Statische Kenndaten ($T_U = 25°C$)		**BD 135**	**BD 137**	**BD 139**	
Kollektor-Emitter-Sättigungsspannung ($I_C = 500$ mA; $I_B = 50$ mA)	U_{CEsat}	< 0,5	< 0,5	< 0,5	V
Kollektor-Basis-Reststrom ($U_{CB} = 30$ V)	I_{CBO}	< 100	< 100	< 100	nA
Kollektor-Basis-Reststrom ($U_{CB} = 30$ V; $T_U = 125°C$)	I_{CBO}	≦ 10	≦ 10	≦ 10	µA
Emitter-Basis-Reststrom ($U_{EB} = 5$ V)	I_{EBO}	≦ 10	≦ 10	≦ 10	µA
Kollektor-Emitter-Durchbruchspannung ($I_{CEO} = 50$ mA)	$U_{(BR)CEO}$	> 45	> 60	> 80	V
Paarungsbedingung ($I_C = 150$ mA; $U_{CE} = 2$ V)	$\frac{B_1}{B_2}$	≦ 1,41	≦ 1,41	≦ 1,41	–
Dynamische Kenndaten ($T_U = 25°C$)					
Transitfrequenz ($I_C = 50$ mA; $U_{CE} = 10$ V; $f = 100$ MHz)	f_T	> 50	> 50	> 50	MHz

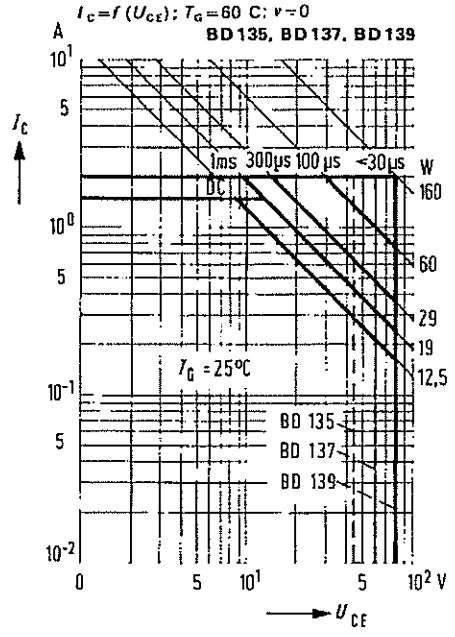
Temperaturabhängigkeit der zulässigen Gesamtverlustleistung
$P_{tot} = f(T)$; R_{th} = Parameter
BD135, BD137, BD139



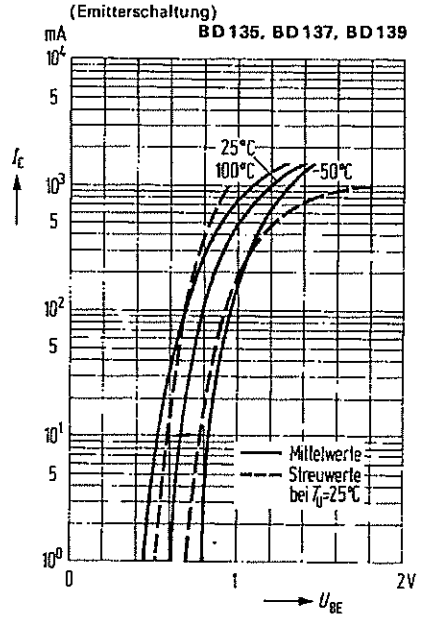
Zulässige Impulsbelastbarkeit
$r_{thJG} = f(t)$; ν = Parameter
BD135, BD137, BD139



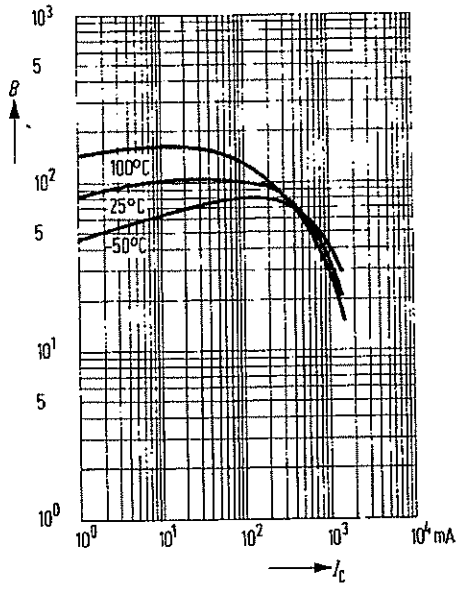
Zulässiger Betriebsbereich
$I_C = f(U_{CE})$; T_G = 60 C; $\nu = 0$
BD135, BD137, BD139



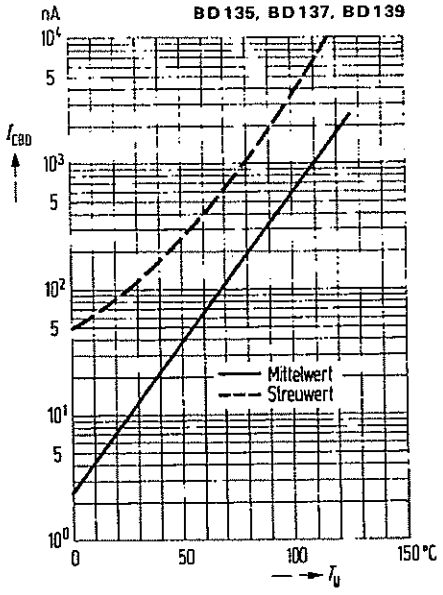
Kollektorstrom $I_C = f(U_{BE})$
U_{CE} = 2 V; T_U = Parameter
(Emitterschaltung)
BD135, BD137, BD139



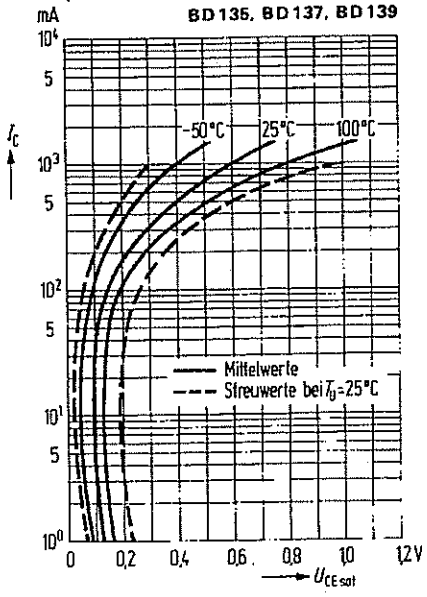
Stromverstärkung $B = f(I_C)$
$U_{CE} = 2$ V; T_U = Parameter
BD 135-10, BD 137-10, BD 139-10



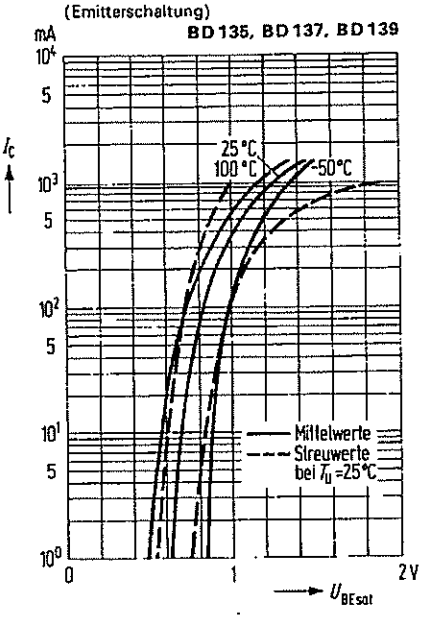
Temperaturabhängigkeit des Reststromes $I_{CBO} = f(T_U)$
BD 135, BD 137, BD 139



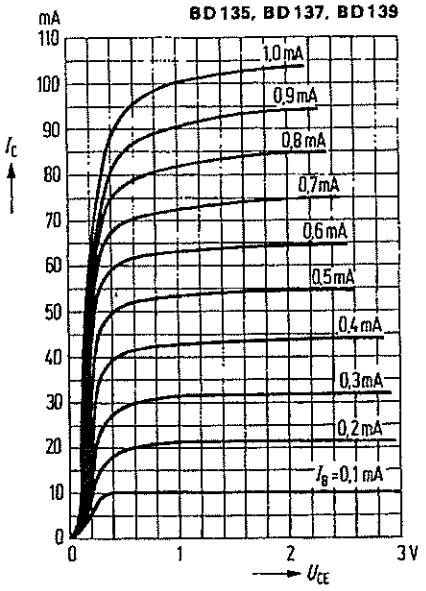
Sättigungsspannung $U_{CEsat} = f(I_C)$
$B = 10$; T_U = Parameter
(Emitterschaltung)
BD 135, BD 137, BD 139



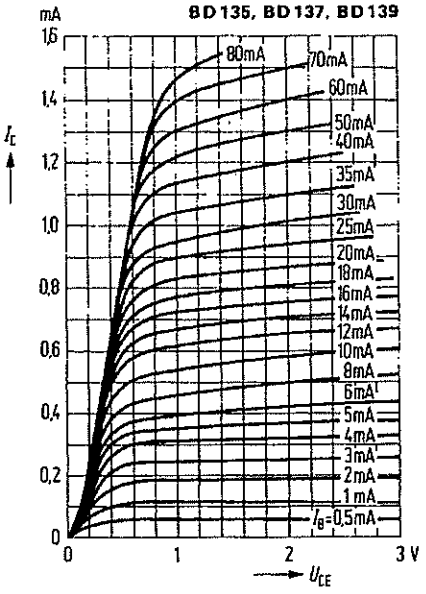
Sättigungsspannung $U_{BEsat} = f(I_C)$
$B = 10$; T_U = Parameter
(Emitterschaltung)
BD 135, BD 137, BD 139



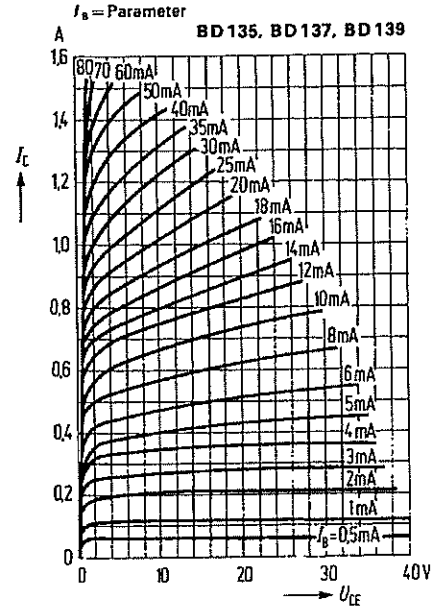
Ausgangskennlinien $I_C = f(U_{CE})$
I_B = Parameter
BD135, BD137, BD139



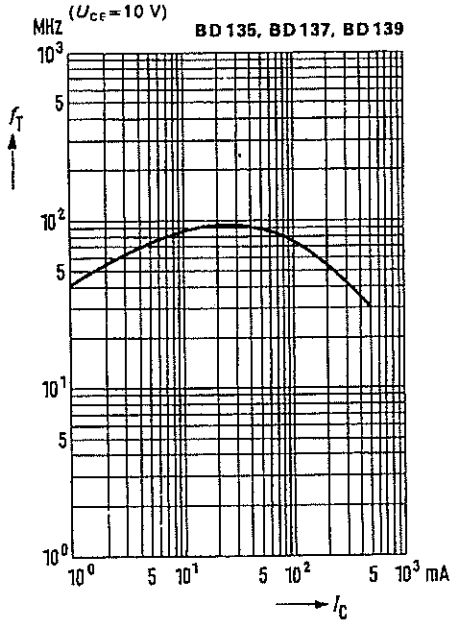
Ausgangskennlinien $I_C = f(U_{CE})$
I_B = Parameter
BD135, BD137, BD139



Ausgangskennlinien $I_C = f(U_{CE})$
I_B = Parameter
BD135, BD137, BD139



Transitfrequenz $f_T = f(I_C)$
(U_{CE} = 10 V)
BD135, BD137, BD139



recommended operating conditions

		SERIES 54 SERIES 74 '09			SERIES 54H SERIES 74H 'H15			SERIES 54LS SERIES 74LS 'LS09, 'LS15			SERIES 54S SERIES 74S 'S09, 'S15			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output voltage, V_{OH}				5.5			5.5			5.5			5.5	V
Low-level output current, I_{OL}	54 Family			16			20			4			20	mA
	74 Family			16			20			8			20	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			SERIES 54 SERIES 74 '09			SERIES 54H SERIES 74H 'H15			SERIES 54LS SERIES 74LS 'LS09, 'LS15			SERIES 54S SERIES 74S 'S09, 'S15			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2				2			2			2			2			V
V_{IL}	Low-level input voltage	1, 2			54 Family			0.8			0.8			0.7			0.8	V
					74 Family			0.8			0.8			0.8			0.8	
V_{IK}	Input clamp voltage	3	V_{CC} = MIN, I_I = §					−1.5			−1.5			−1.5			−1.2	V
I_{OH}	High-level output current	1	V_{CC} = MIN, V_{IH} = 2 V, V_{OH} = 5.5 V,					250			250			100			250	μA
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V	I_{OL} = MAX	54 Family		0.2	0.4		0.15	0.3		0.25	0.4			0.5	V
					74 Family		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
				I_{OL} = 4 mA	Series 74LS								0.25	0.4				
I_I	Input current at maximum input voltage	4	V_{CC} = MAX		V_I = 5.5 V			1			0.1						1	mA
					V_I = 7 V									0.1				
I_{IH}	High-level input current	4	V_{CC} = MAX		V_{IH} = 2.4 V			40			50							μA
					V_{IH} = 2.7 V									20			50	
I_{IL}	Low-level input current	5	V_{CC} = MAX		V_{IL} = 0.4 V			−1.6			−2			−0.4				mA
					V_{IL} = 0.5 V												−2	
I_{CC}	Supply current	7	V_{CC} = MAX			See table on next page												mA

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§I_I = − 12 mA for SN54'/SN74', −8 mA for SN54H'/SN74H', and −18 mA for SN54LS'/SN74LS'.

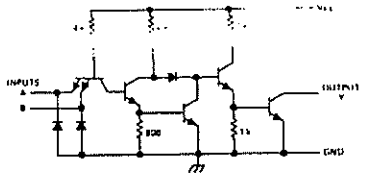
TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'09	11	21	20	33	3.88
'H15	15	25	30	48	7.5
'LS09	2.4	4.8	4.4	8.8	0.85
'LS15	1.8	3.6	3.3	6.6	0.85
'S09	18	32	32	57	6.25
'S15	10.5	19.5	24	42	5.75

¶Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A, typical values are at V_{CC} = 5 V, T_A = 25° C.

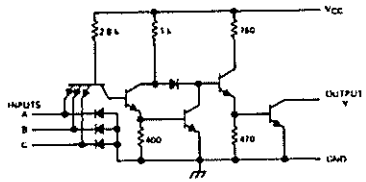
switching characteristics at V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'09	C_L = 15 pF, R_L = 400 Ω		21	32		16	24
'H15	C_L = 25 pF, R_L = 280 Ω		12	18		9	13
'LS09, 'LS15	C_L = 15 pF, R_L = 2 kΩ		20	35		17	35
'S09	C_L = 15 pF, R_L = 280 Ω		6.5	10		6.5	10
	C_L = 50 pF, R_L = 280 Ω		9			9	
'S15	C_L = 15 pF, R_L = 280 Ω		5.5	8.5		6	9
	C_L = 50 pF, R_L = 280 Ω		8.5			8	

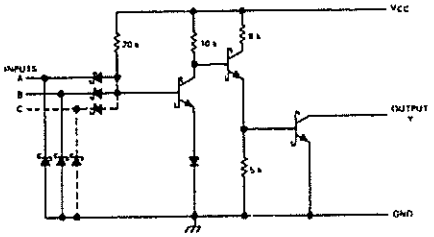
#Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.



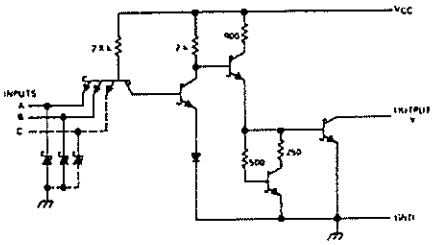
'09 CIRCUITS



'H15 CIRCUITS



'LS09, 'LS15 CIRCUITS



'S09, 'S15 CIRCUITS

Resistor values shown are nominal and in ohms.

recommended operating conditions

		SERIES 54S/74S	'574			'5112			'5113			'5114			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		Series 54S	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		Series 74S	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−1			−1			−1			−1	mA
Low-level output current, I_{OL}					20			20			20			20	mA
Pulse width, t_w	Clock high		6			6			6			6			ns
	Clock low		7.3			6.5			6.5			6.5			
	Clear or preset low		7			8			8			8			
Input setup time, t_{su}	High-level data		3↑			3↓			3↓			3↓			ns
	Low-level data		3↑			3↓			3↓			3↓			
Input hold time, t_h			2↑			0↓			0↓			0↓			ns
Operating free-air temperature, T_A		Series 54S	−55		125	−55		125	−55		125	−55		125	°C
		Series 74S	0		70	0		70	0		70	0		70	

†↓The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	'574			'5112			'5113			'5114			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2			−1.2			−1.2	V
V_{OH}	High-level output voltage	Series 54S	V_{CC} = MIN, V_{IH} = 2 V,	2.5	3.4		2.5	3.4		2.5	3.4		2.5	3.4		V
		Series 74S	V_{IL} = 0.8 V, I_{OH} = −1 mA	2.7	3.4		2.7	3.4		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.5			0.5			0.5			0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1			1			1	mA
I_{IH}	High-level input current	J, K, or D	V_{CC} = MAX, V_I = 2.7 V			50			50			50			50	μA
		Clear				150			100						200	
		Preset				100			100			100			100	
		Clock				100			100			100			200	
I_{IL}	Low-level input current	J, K, or D	V_{CC} = MAX, V_I = 0.5 V			−2			−1.6			−1.6			−1.6	mA
		Clear ★				−6			−7						−14	
		Preset ★				−4			−7			−7			−7	
		Clock				−4			−4			−4			−8	
I_{OS}	Short-circuit output current¶		V_{CC} = MAX	−40		−100	−40		−100	−40		−100	−40		−100	mA
I_{CC}	Supply current (average per flip-flop)		V_{CC} = MAX, See Note 1		15	25		15	25		15	25		15	25	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

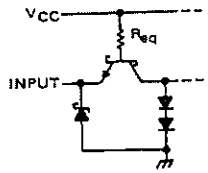
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'S74 MIN	'S74 TYP	'S74 MAX	'S112, 'S113, 'S114 MIN	'S112, 'S113, 'S114 TYP	'S112, 'S113, 'S114 MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 280 Ω, See Note 2	75	110		80	125		MHz
t_{PLH}	Preset or clear	Q or $\overline{Q}$			4	6		4	7	ns
t_{PHL}	Preset or clear (clock high)	$\overline{Q}$ or Q			9	13.5		5	7	ns
	Preset or clear (clock low)				5	8		5	7	
t_{PLH}	Clock	Q or $\overline{Q}$			6	9		4	7	ns
t_{PHL}					6	9		5	7	

¶ f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 2: Load circuit and voltage waveforms are shown on page 3-10.

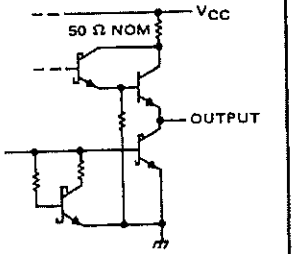
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

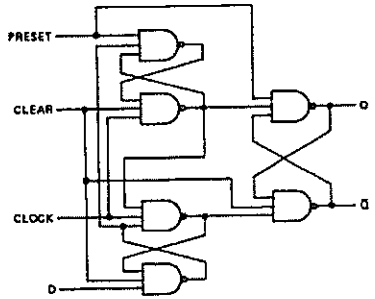


I_{IL} MAX	R_{eq} NOM
−1.6 mA	4 kΩ
−2 mA	2.8 kΩ
−4 mA	1.4 kΩ
−6 mA	940 Ω
−7 mA	900 Ω
−8 mA	700 Ω
−14 mA	450 Ω

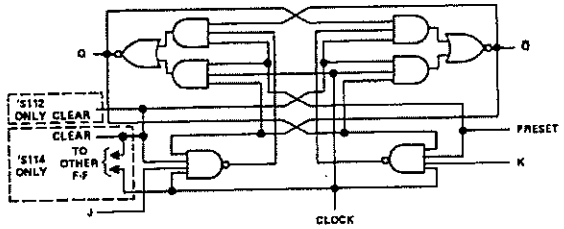
TYPICAL OF ALL OUTPUTS



functional block diagrams



'S74—DUAL D WITH CLEAR AND PRESET



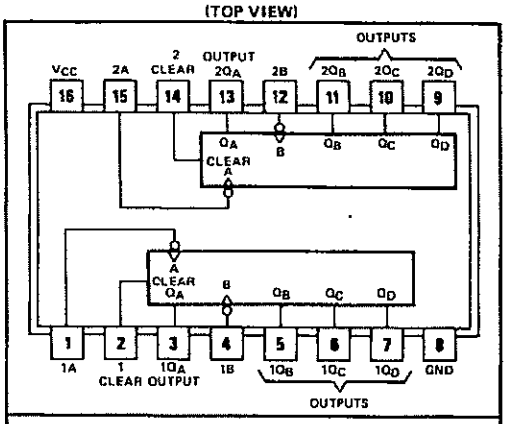
'S112—DUAL J-K WITH CLEAR AND PRESET
'S113—DUAL J-K WITH PRESET
'S114—DUAL J-K WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

TYPES SN54390, SN54LS390, SN54393, SN54LS393, SN74390, SN74LS390, SN74393, SN74LS393
DUAL 4-BIT DECADE AND BINARY COUNTERS

BULLETIN NO. DL-S 7612099, OCTOBER 1976

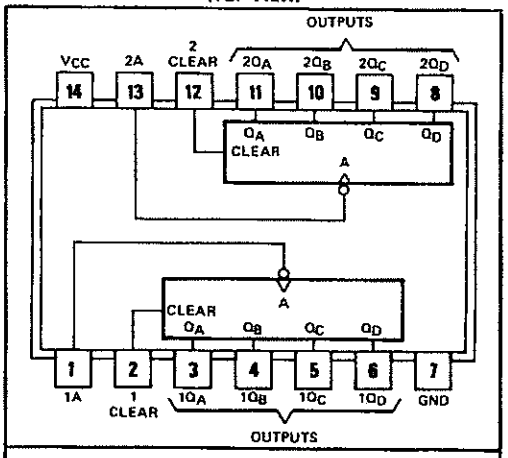
- Versions of the Popular '90A, 'LS90 '93A, 'LS93
- 'LS390. . .Individual Clocks for A and B Flops Provide Dual ÷2 and ÷5 Counters
- 'LS393. . .Dual 4-Bit Binary Counter Individual Clocks
- Have Direct Clear for Each Counter
- 4-Bit Versions Can Significantly Improve System Densities by Reducing Counter Package Count by 50%
- Typical Maximum Count Frequency . . . 35 MHz
- Buffered Outputs Reduce Possibility of Collector Commutation

SN54390, SN54LS390 . . . J OR W PACKAGE
SN74390, SN74LS390 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: High input to clear resets all four outputs low

SN54393, SN54LS393 . . . J OR W PACKAGE
SN74393, SN54LS393 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: High input to clear resets all four outputs low

of these monolithic circuits contains eight slave flip-flops and additional gating to implete two individual four-bit counters in a single . The '390 and 'LS390 incorporate dual by-two and divide-by-five counters, which can d to implement cycle lengths equal to any and/or cumulative multiples of 2 and/or 5 up ide-by-100. When connected as a bi-quinary r, the separate divide-by-two circuit can be provide symmetry (a square wave) at the final stage. The '393 and 'LS393 each comprise dependent four-bit binary counters each having and a clock input. N-bit binary counters can plemented with each package providing the ity of divide-by-256. The '390, 'LS390, '393, S393 have parallel outputs from each counter so that any submultiple of the input count ncy is available for system-timing signals.

54 and Series 54LS circuits are characterized ration over the full military temperature range °C to 125°C; Series 74 and Series 74LS are characterized for operation from 0°C C.

FUNCTION TABLES

'390, 'LS390
BCD COUNT SEQUENCE
(EACH COUNTER)
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'390, 'LS390
BI-QUINARY (5-2)
(EACH COUNTER)
(See Note B)

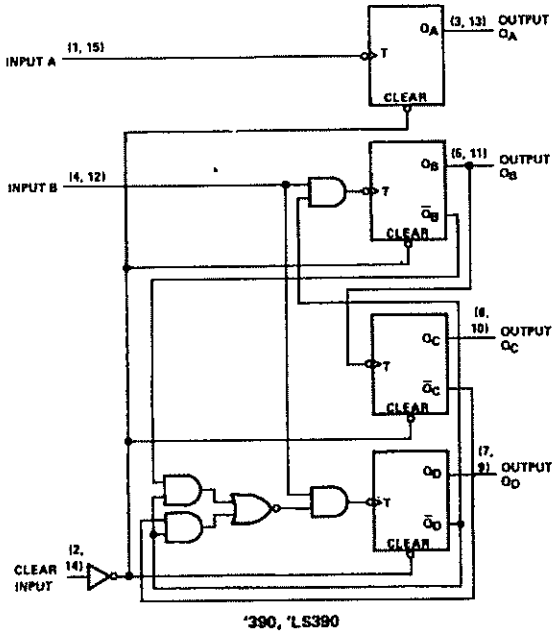
COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'393, 'LS393
COUNT SEQUENCE
(EACH COUNTER)

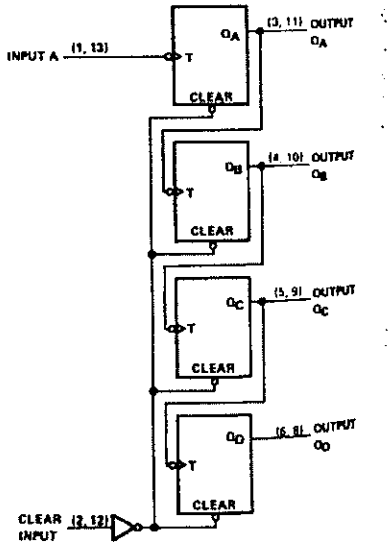
COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTES: A. Output Q_A is connected to Input B for BCD count.
B. Output Q_D is connected to Input A for bi-quinary count.
C. H = high level, L = low level.

functional block diagrams



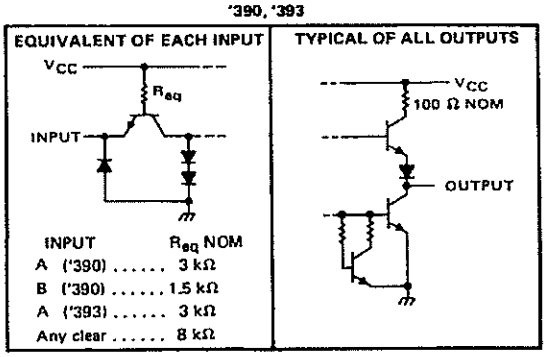
'390, 'LS390



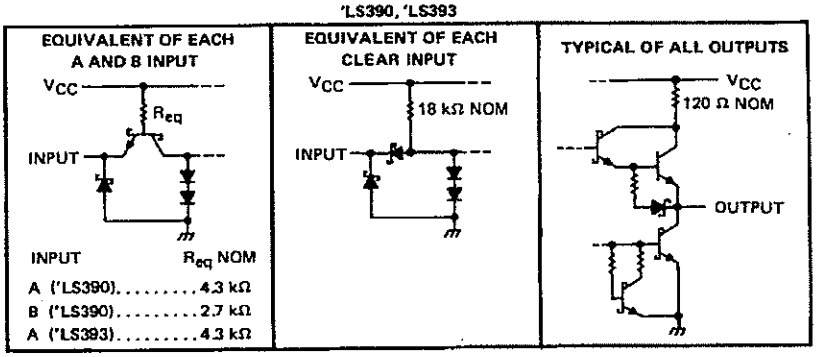
'393, 'LS393

of inputs and outputs

'390, '393



'LS390, 'LS393



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54390, SN54393 . . . . . −55°C to 125°C
SN74390, SN74393 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54390 SN54393			SN74390 SN74393			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Count frequency, f_{count}	A input	0		25	0		25	MHz
	B input	0		20	0		20	
Pulse width, t_w	A input high or low	20			20			ns
	B input high or low	25			25			
	Clear high	20			20			
Clear inactive-state setup time, t_{su}		25↓			25↓			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

↓ The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		'390 MIN	'390 TYP‡	'390 MAX	'393 MIN	'393 TYP	'393 MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA¶			0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	Clear	V_{CC} = MAX, V_I = 2.4 V				40			40	μA
		Input A					80			80	
		Input B					120				
I_{IL}	Low-level input current	Clear	V_{CC} = MAX, V_I = 0.4 V				−1			−1	mA
		Input A					−3.2			−3.2	
		Input B					−4.8				
I_{OS}	Short-circuit output current§		V_{CC} = MAX	SN54'	−20		−57	−20		−57	mA
				SN74'	−18		−57	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX, See Note 2			42	69		38	64	mA

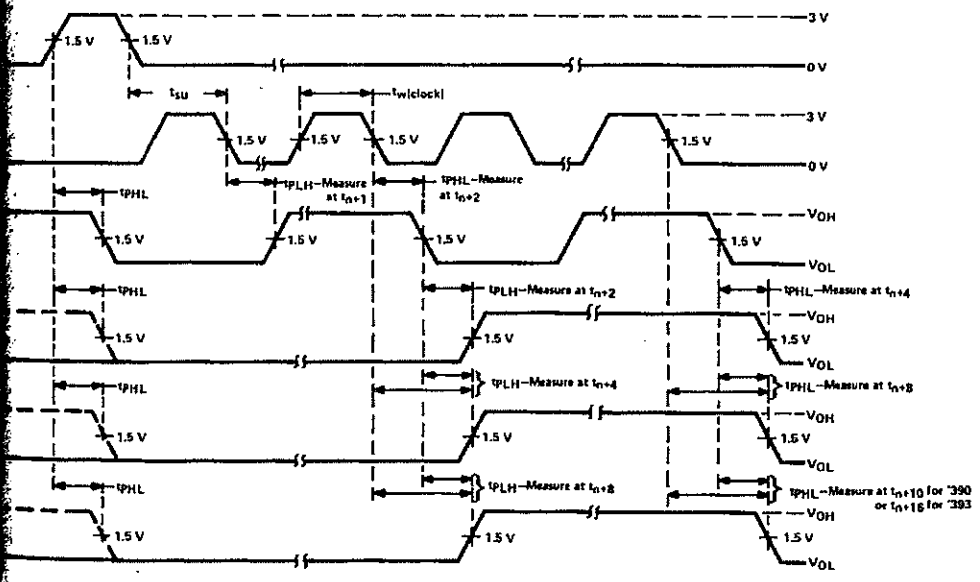
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶ The Q_A outputs of the '390 are tested at I_{OL} = 16 mA plus the limit value for I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.
§ Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'390			'393			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	A	Q_A	C_L = 15 pF, R_L = 400 Ω, See Note 3 and Figure 1	25	35		25	35		MHz
	B	Q_B		20	30					
t_{PLH}	A	Q_A			12	20		12	20	ns
t_{PHL}					13	20		13	20	
t_{PLH}	A	Q_C of '390 Q_D of '393			37	60		40	60	ns
t_{PHL}					39	60		40	60	
t_{PLH}	B	Q_B			13	21				ns
t_{PHL}					14	21				
t_{PLH}	B	Q_C			24	39				ns
t_{PHL}					26	39				
t_{PLH}	B	Q_D			13	21				ns
t_{PHL}					14	21				
t_{PHL}	Clear	Any			24	39		24	39	ns

imum count frequency
pagation delay time, low-to-high-level output
pagation delay time, high-to-low level output
d circuit is shown on page 3-10.

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

ut pulses are supplied by a generator having the following characteristics $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $_{out}$ ≈ 50 ohms.

FIGURE 1

TYPES SN5446A, '47A, '48, '49, SN54L46, 'L47, SN54LS47, 'LS48, SN7446A, '47A, '48, SN74L46, 'L47, SN74LS47, 'LS48, BCD-TO-SEVEN-SEGMENT DECODERS/DR

BULLETIN NO. DL-S 7611811, MARCH 1974—REVISED OCTO

'46A, '47A, 'L46, 'L47, 'LS47 feature

- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

'48, 'LS48 feature

- Internal Pull-Ups Eliminate Need for External Resistors
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

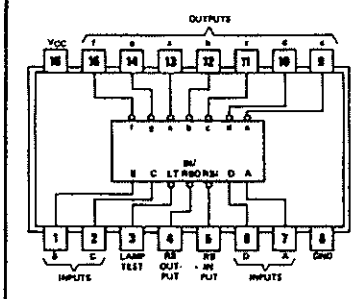
'49, 'LS49 feature

- Open-Collector Outp
- Blanking Input

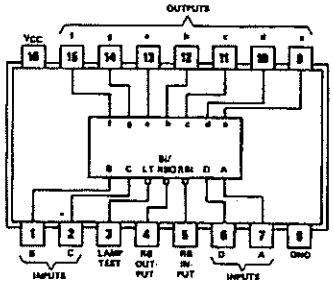
- All Circuit Types Feature Lamp Intensity Modulation Capability

TYPE	DRIVER OUTPUTS				TYPICAL POWER DISSIPATION	PACKAGES
	ACTIVE LEVEL	OUTPUT CONFIGURATION	SINK CURRENT	MAX VOLTAGE		
SN5446A	low	open-collector	40 mA	30 V	320 mW	J, W
SN5447A	low	open-collector	40 mA	15 V	320 mW	J, W
SN5448	high	2-kΩ pull-up	6.4 mA	5.5 V	265 mW	J, W
SN5449	high	open-collector	10 mA	5.5 V	165 mW	W
SN54L46	low	open-collector	20 mA	30 V	160 mW	J
SN54L47	low	open-collector	20 mA	15 V	160 mW	J
SN54LS47	low	open-collector	12 mA	15 V	35 mW	J, W
SN54LS48	high	2-kΩ pull-up	2 mA	5.5 V	125 mW	J, W
SN54LS49	high	open-collector	4 mA	5.5 V	40 mW	J, W
SN7446A	low	open-collector	40 mA	30 V	320 mW	J, N
SN7447A	low	open-collector	40 mA	15 V	320 mW	J, N
SN7448	high	2-kΩ pull-up	6.4 mA	5.5 V	265 mW	J, N
SN74L46	low	open-collector	20 mA	30 V	160 mW	J, N
SN74L47	low	open-collector	20 mA	15 V	160 mW	J, N
SN74LS47	low	open-collector	24 mA	15 V	35 mW	J, N
SN74LS48	high	2-kΩ pull-up	6 mA	5.5 V	125 mW	J, N
SN74LS49	high	open-collector	8 mA	5.5 V	40 mW	J, N

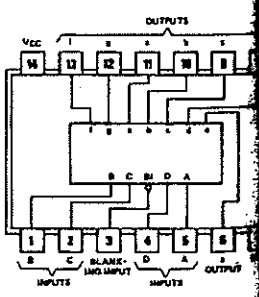
'46A, '47A, 'L46, 'L47, 'LS47 (TOP VIEW)



'48, 'LS48 (TOP VIEW)



'49, 'LS49 (TOP VIEW)



positive logic: see function tables

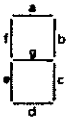
TYPES SN5446A, '47A, '48, '49, SN54L46, 'L47, SN54LS47, 'LS48, 'LS49, SN7446A, '47A, '48, SN74L46, 'L47, SN74LS47, 'LS48, 'LS49 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

ion

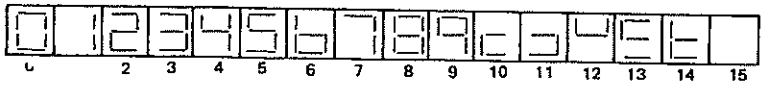
'46A, 'L46, '47A, 'L47, and 'LS47 feature active-low outputs designed for driving common-anode VLEDs or ndescent indicators directly, and the '48, '49, 'LS48, 'LS49 feature active-high outputs for driving lamp buffers or mmon-cathode VLEDs. All of the circuits except '49 and 'LS49 have full ripple-blanking input/output controls and a p test input. The '49 and 'LS49 circuits incorporate a direct blanking input. Segment identification and resultant plays are shown below. Display patterns for BCD input counts above 9 are unique symbols to authenticate input nditions.

'46A, '47A, '48, 'L46, 'L47, 'LS47, and 'LS48 circuits incorporate automatic leading and/or trailing-edge o-blanking control (RBI and RBO). Lamp test (LT) of these types may be performed at any time when the BI/RBO e is at a high level. All types (including the '49 and 'LS49) contain an overriding blanking input (BI) which can be d to control the lamp intensity by pulsing or to inhibit the outputs. Inputs and outputs are entirely compatible for with TTL or DTL logic outputs.

SN54246/SN74246 through '249 and the SN54LS247/SN74LS247 through 'LS249 compose the 6 and 9 with tails and have been designed to offer the designer a choice between two indicator fonts. The 4249/SN74249 and SN54LS249/SN74LS249 are 16-pin versions of the 14-pin SN5449 and 'LS49. Included in the circuit and 'LS249 circuits are the full functional capability for lamp test and ripple blanking, which is available in the '49 or 'LS49 circuit.



SEGMENT IDENTIFICATION



NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

'46A, '47A, 'L46, 'L47, 'LS47 FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	1
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	OFF	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

…el, L = low level, X = irrelevant

…s: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are off regardless of the level of any other input.
3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

…wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

'48, 'LS48
FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

H = high level, L = low level, X = irrelevant

NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are d
ripple-blanking input (RBI) must be open or high, if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the l
other input.
3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp-test input high, all segm
go low and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple-blanking output (BI/RBO) is open or held high and a low is applied to the lamp-te
segment outputs are high.

†BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

'49, 'LS49
FUNCTION TABLE

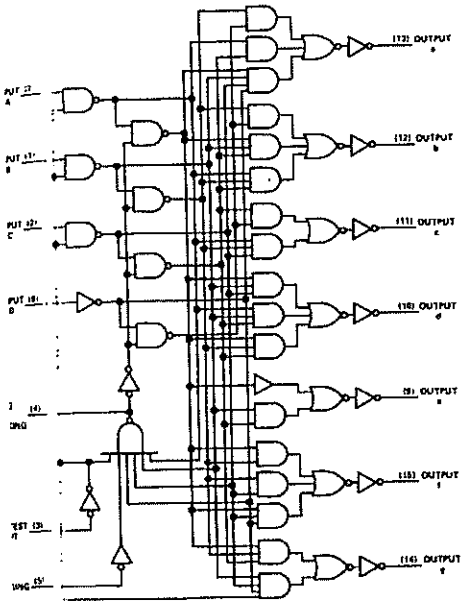
DECIMAL OR FUNCTION	INPUTS					OUTPUTS							NOTE
	D	C	B	A	BI	a	b	c	d	e	f	g	
0	L	L	L	L	H	H	H	H	H	H	H	L	1
1	L	L	L	H	H	L	H	H	L	L	L	L	
2	L	L	H	L	H	H	H	L	H	H	L	H	
3	L	L	H	H	H	H	H	H	H	L	L	H	
4	L	H	L	L	H	L	H	H	L	L	H	H	
5	L	H	L	H	H	H	L	H	H	L	H	H	
6	L	H	H	L	H	L	L	H	H	H	H	H	
7	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	L	L	L	L	L	L	L	L	2

H = high level, L = low level, X = irrelevant

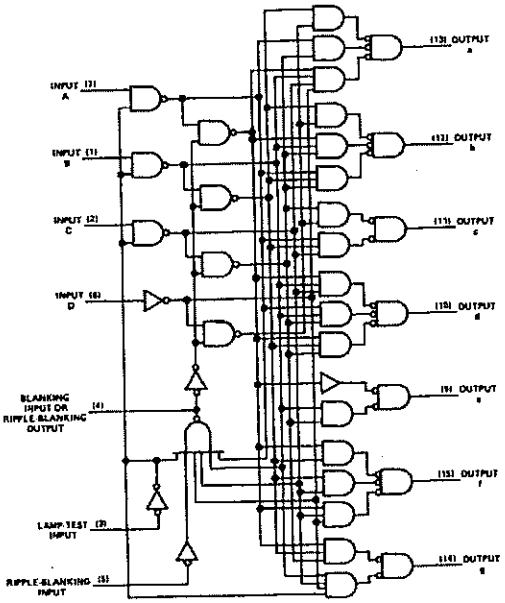
NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the l
other input.

ɔnal block diagrams

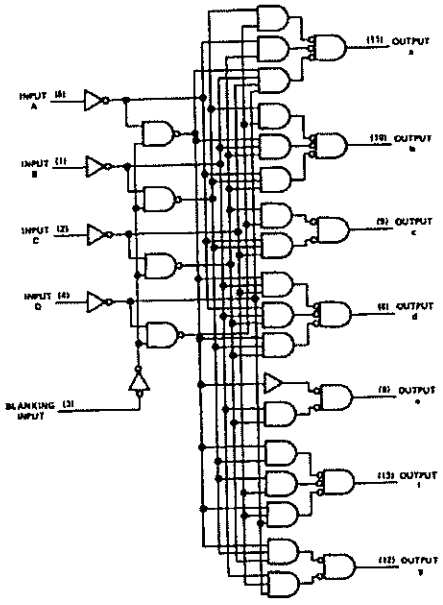
'46A, '47A, 'L46, 'L47, 'LS47



'48, 'LS48



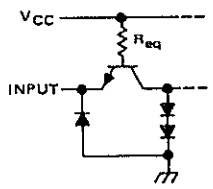
'48, 'LS49



schematics of inputs and outputs

'46A, '47A, '48, '49, 'L46, 'L47

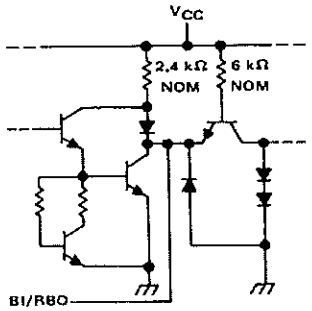
EQUIVALENT OF EACH INPUT EXCEPT BI/RBO



SN54'/SN74': R_{eq} = 6 kΩ NOM
SN54L'/SN74L': R_{eq} = 8 kΩ NOM

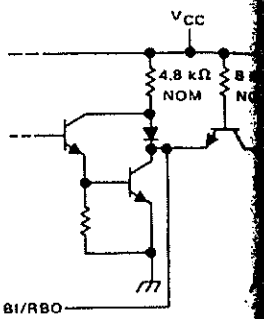
'46A, '47A, '48

EQUIVALENT OF BI/RBO



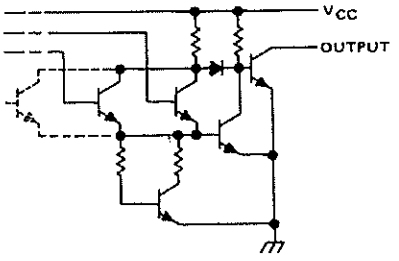
'L46, 'L47

EQUIVALENT OF BI/RBO



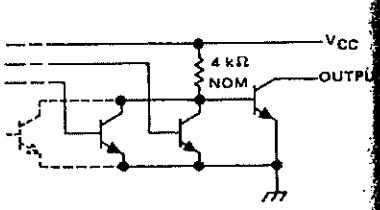
'46A, '47A

TYPICAL OF OUTPUTS a THRU g



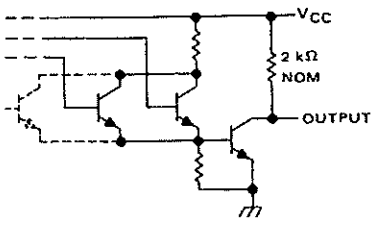
'L46, 'L47

TYPICAL OF OUTPUTS a THRU g



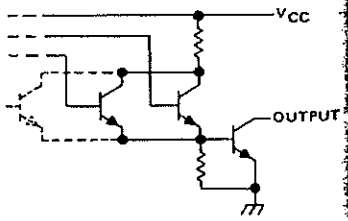
'48

TYPICAL OF OUTPUTS a THRU g



'49

TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . .
Input voltage . . . .
Current forced into any output in the off state . . . .
Operating free-air temperature range: SN5446A, SN5447A . . . . −55°C
SN7446A, SN7447A . . . . 0°C
Storage temperature range . . . . −65°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN5446A			SN5447A			SN7446A			SN7447A		
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX
Supply voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25
Off-state output voltage, $V_{O(off)}$	a thru g			30			15			30			
On-state output current, $I_{O(on)}$	a thru g			40			40			40			
High-level output current, I_{OH}	BI/RBO			−200			−200			−200			−200
Low-level output current, I_{OL}	BI/RBO			8			8			8			
Operating free-air temperature, T_A		−55		125	−55		125	0		70	0		

electrical characteristics over recommended operating free-air temperature range (unless otherwise n

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MA
V_{IH}	High-level input voltage				2		
V_{IL}	Low-level input voltage						0.
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.
V_{OH}	High-level output voltage	BI/RBO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −200 μA		2.4	3.7	
V_{OL}	Low-level output voltage	BI/RBO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 8 mA			0.27	0.
$I_{O(off)}$	Off-state output current	a thru g	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, $V_{O(off)}$ = MAX				25
$V_{O(on)}$	On-state output voltage	a thru g	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, $I_{O(on)}$ = 40 mA			0.3	0.
I_I	Input current at maximum input voltage	Any input except BI/RBO	V_{CC} = MAX, V_I = 5.5 V				
I_{IH}	High-level input current	Any input except BI/RBO	V_{CC} = MAX, V_I = 2.4 V				
I_{IL}	Low-level input current	Any input except BI/RBO	V_{CC} = MAX, V_I = 0.4 V				−1.
		BI/RBO					−.
I_{OS}	Short-circuit output current	BI/RBO	V_{CC} = MAX				−.
I_{CC}	Supply current		V_{CC} = MAX, See Note 2	SN54'		64	
				SN74'		64	10

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MA
t_{off}	Turn-off time from A input	C_L = 15 pF, R_L = 120 Ω, See Note 3			10
t_{on}	Turn-on time from A input				10
t_{off}	Turn-off time from RBI input				10
t_{on}	Turn-on time from RBI input				10

NOTE 3: Load circuit and voltage waveforms are shown on page 3-10; t_{off} corresponds to t_{PLH} and t_{on} corresponds to t_{PHL}.

DATA SHEET

74F30
8-input NAND gate

Product specification

1989 Mar 03

IC15 Data Handbook

Philips
Semiconductors

PHILIPS

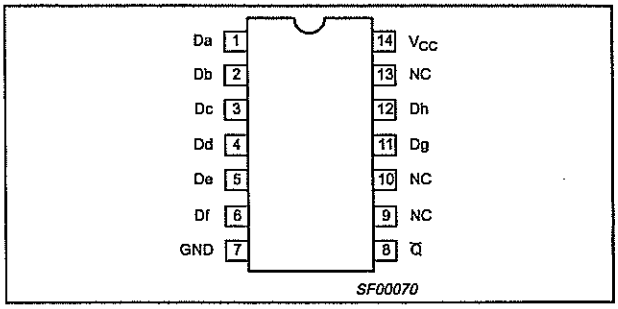
8-input NAND gate | 74F30

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F30	3.2ns	1.7mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
14-pin plastic DIP	N74F30N	SOT27-1
14-pin plastic SO	N74F30D	SOT108-1

PIN CONFIGURATION

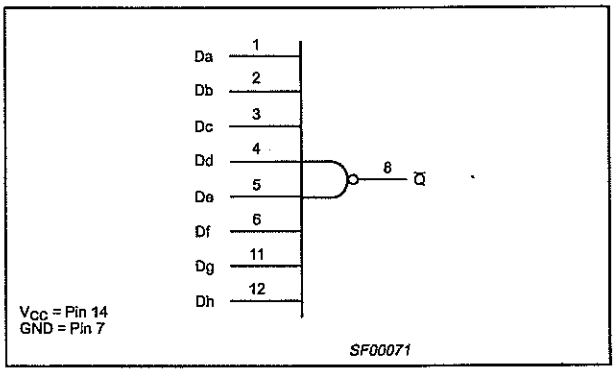


INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dn	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}$	Data output	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

LOGIC DIAGRAM

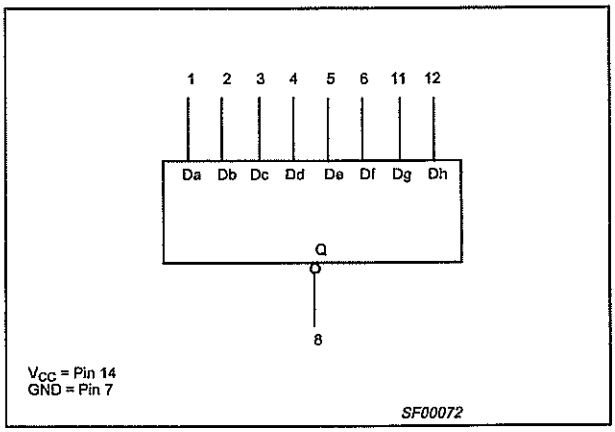


FUNCTION TABLE

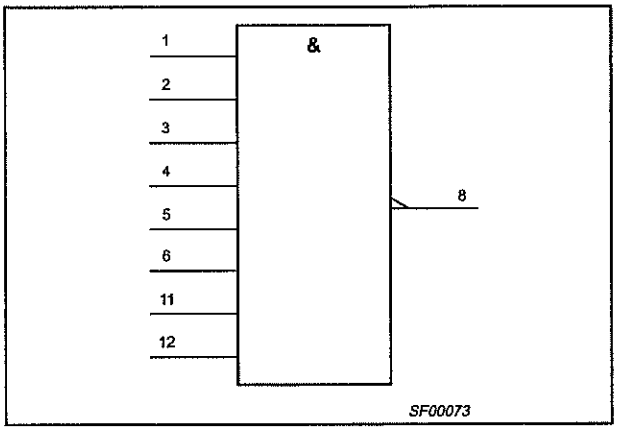
INPUTS								OUTPUT
Dna	Dnb	Dnc	Dnd	Dne	Dnf	Dng	Dnh	$\overline{Q}$n
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

NOTES:
1. H = High voltage level
2. L = Low voltage level
3. X = Don't care

LOGIC SYMBOL



IEC/IEEE SYMBOL



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} = GND		0.6	1.5	mA
		I_{CCL}		V_{IN} = 4.5V		2.8	4.0	

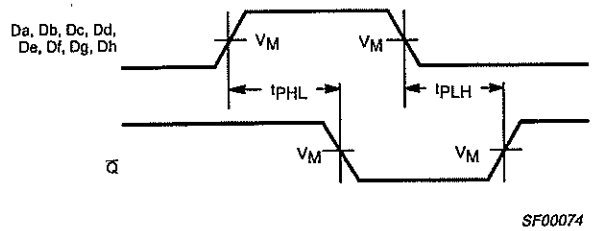
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Da, Db, Dc, Dd, De, Df, Dg, Dh to $\overline{Q}$	Waveform 1	1.5 1.0	3.5 3.0	5.0 4.5	1.5 1.0	5.5 5.0	ns

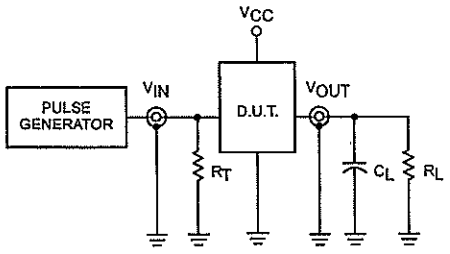
AC WAVEFORMS



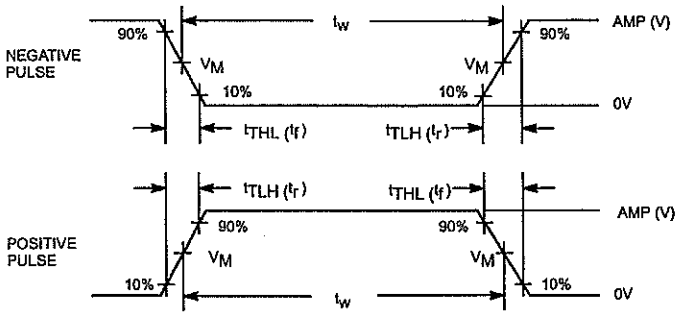
Waveform 1. Propagation Delay for Inverting Outputs

NOTE:
For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

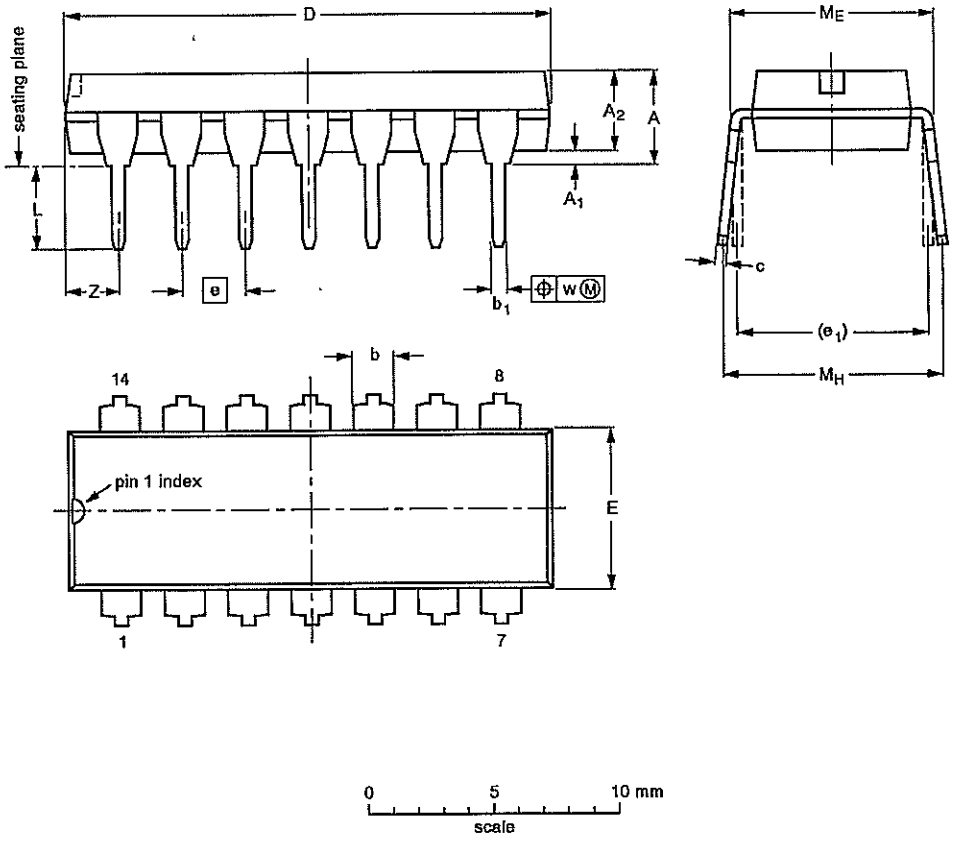
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

DIP14: plastic dual in-line package; 14 leads (300 mil) SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

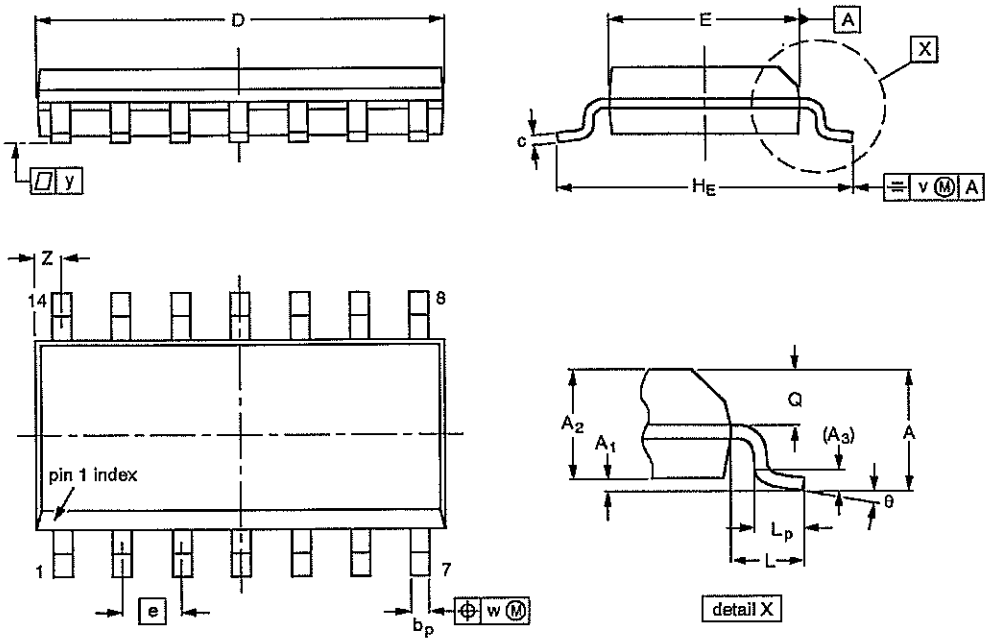
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

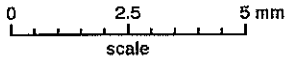
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				~~92-11-17~~ 95-03-11

SO14: plastic small outline package; 14 leads; body width 3.9 mm SOT108-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				~~95-01-23~~ 97-05-22

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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DATA SHEET

74ABT00
Quad 2-input NAND gate

Product specification

IC23 Data Handbook

1995 Sep 18

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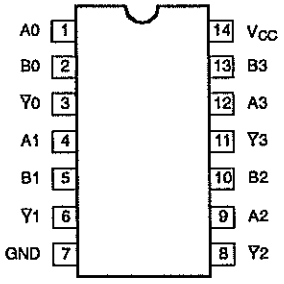
Quad 2-input NAND gate | 74ABT00

JICK REFERENCE DATA

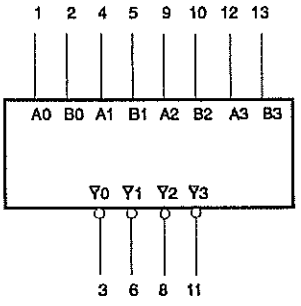
YMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An or Bn to $\overline{Y}n$	C_L = 50pF; V_{CC} = 5V	2.5 2.0	ns
t_{OSLH} t_{OSHL}	Output to Output skew		0.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
I_{CC}	Total supply current	Outputs disabled; V_{CC} = 5.5V	50	µA

N CONFIGURATION



SA00333

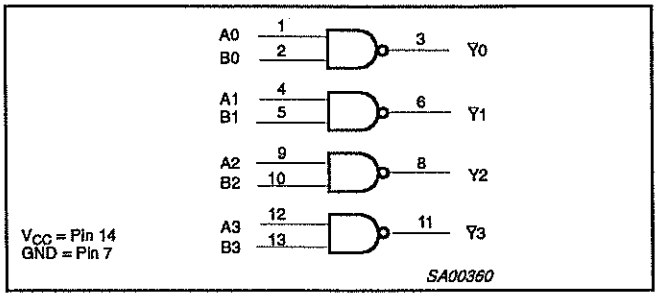
OGIC SYMBOL



VCC = Pin 14
GND = Pin 7

SA00334

LOGIC DIAGRAM



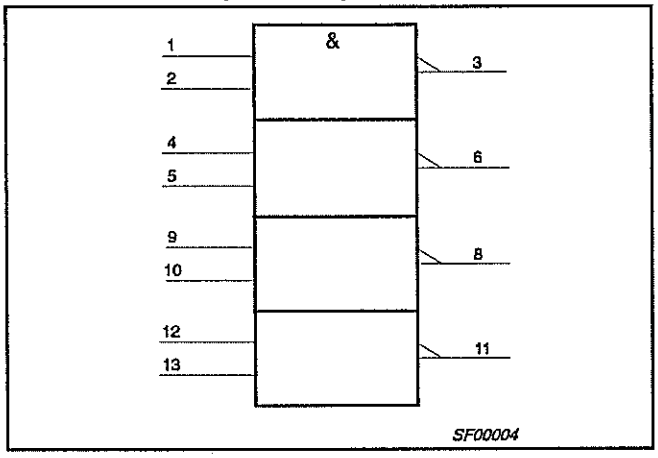
VCC = Pin 14
GND = Pin 7

SA00360

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 4, 5, 9, 10, 12, 13	An-Bn	Data inputs
3, 6, 8, 11	$\overline{Y}n$	Data outputs
7	GND	Ground (0V)
14	V_{CC}	Positive supply voltage

LOGIC SYMBOL (IEEE/IEC)



SF00004

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

NOTES:
H = High voltage level
L = Low voltage level

RDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
4-Pin Plastic DIP	–40°C to +85°C	74ABT00 N	74ABT00 N	SOT27-1
4-Pin plastic SO	–40°C to +85°C	74ABT00 D	74ABT00 D	SOT108-1
4-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT00 DB	74ABT00 DB	SOT337-1
4-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT00 PW	74ABT00PW DH	SOT402-1

SOLUTE MAXIMUM RATINGS[1, 2]

YMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage[3]		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	40	mA
T_{stg}	Storage temperature range		−65 to 150	°C

TES:
Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

ECOMMENDED OPERATING CONDITIONS

YMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−15	mA
I_{OL}	Low-level output current		20	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

C ELECTRICAL CHARACTERISTICS

YMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = −40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = −18mA		−0.9	−1.2		−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = −15mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 20mA; V_I = V_{IL} or V_{IH}		0.35	0.5		0.5	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or V_I ≤ 4.5V		±5.0	±100		±100	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	−50	−75	−180	−50	−180	mA
I_{CC}	Quiescent supply current	V_{CC} = 5.5V; V_I = GND or V_{CC}		2	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One data input at 3.4V, other inputs at V_{CC} or GND		0.25	500		500	µA

TES:
Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
This is the increase in supply current for each input at 3.4V.

C CHARACTERISTICS

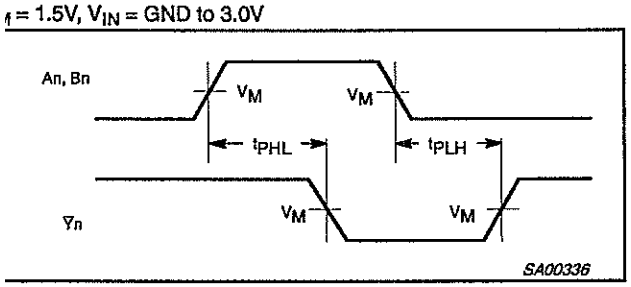
ID = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An or Bn to $\overline{Y}$n	1	1.0 1.0	2.5 2.0	3.6 2.8	1.0 1.0	4.1 3.4	ns
t_{OSHL} t_{OSLH}[1]	Output to Output skew An or Bn to $\overline{Y}$n	2		0.4 0.4	0.5 0.5		0.5 0.5	ns

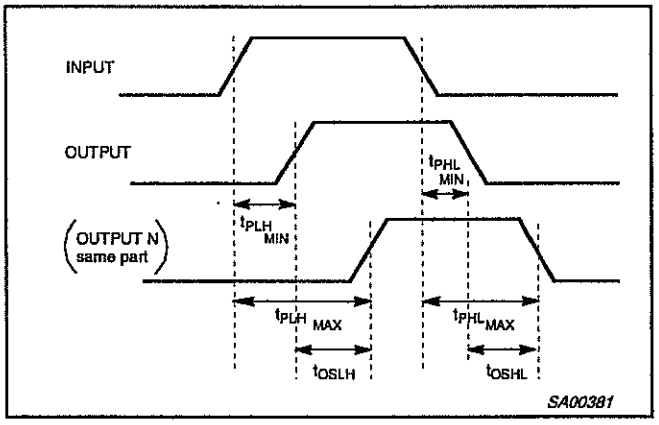
TE:
Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

C WAVEFORMS

= 1.5V, V_{IN} = GND to 3.0V

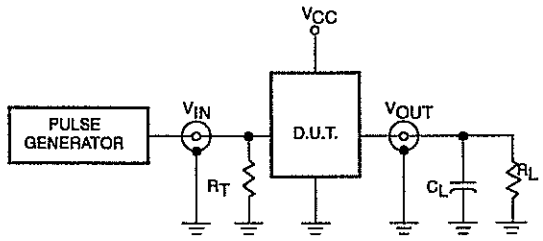


Waveform 1. Propagation delay for inverting outputs

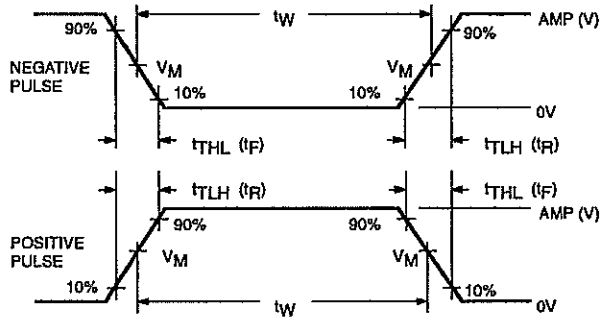


Waveform 2. Common edge skew

EST CIRCUIT AND WAVEFORMS



Test Circuit for Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

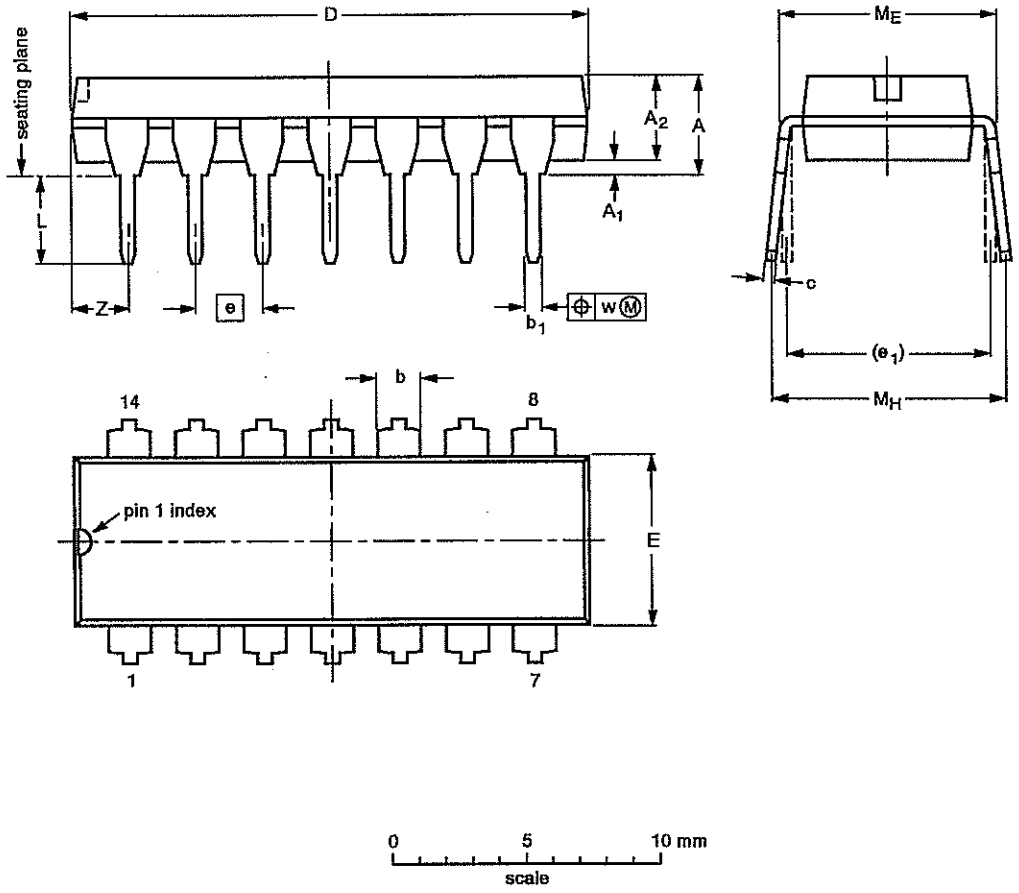
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SH00067

P14: plastic dual in-line package; 14 leads (300 mil) SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				~~92-11-17~~ 95-03-11

DATA SHEET

74F273A
Octal D flip-flop

Product specification

1996 Mar 12

IC15 Data Handbook

Philips
Semiconductors

PHILIPS

Octal D-type flip-flop 74ABT273A

:ATURES

:ight edge-triggered D-type flip-flops

3uffered common clock

3uffered asynchronous Master Reset

?ower-up reset

3ee 74ABT377 for clock enable version

3ee 74ABT373 for transparent latch version

3ee 74ABT374 for 3-State version

:SD protection exceeds 2000 V per Mil Std 833 Method 3015 and 200 V per machine model.

DESCRIPTION

The 74ABT273A has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced Low independent of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the CP and $\overline{MR}$ are common elements.

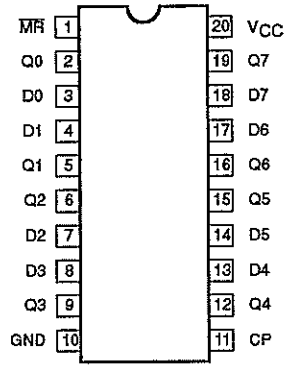
UICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 5V	3.0 3.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	pF
I_{CCH}	Total supply current	Outputs High; V_{CC} =5.5V	150	µA

RDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
0-Pin Plastic DIP	–40°C to +85°C	74ABT273A N	74ABT273A N	SOT146-1
0-Pin plastic SO	–40°C to +85°C	74ABT273A D	74ABT273A D	SOT163-1
0-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT273A DB	74ABT273A DB	SOT339-1
0-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT273A PW	7ABT273APW DH	SOT360-1

IN CONFIGURATION

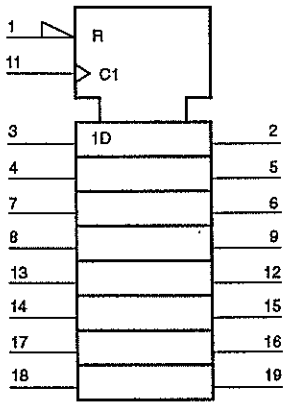


PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
11	CP	Clock pulse input (active rising edge)
3, 4, 7, 8, 13, 14, 17, 18	D0 - D7	Data inputs
2, 5, 6, 9, 12, 15, 16, 19	Q0 - Q7	Data outputs
1	$\overline{MR}$	Master Reset input (active-Low)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

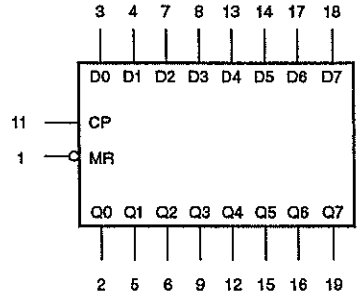
Octal D-type flip-flop 74ABT273A

)GIC SYMBOL (IEEE/IEC)



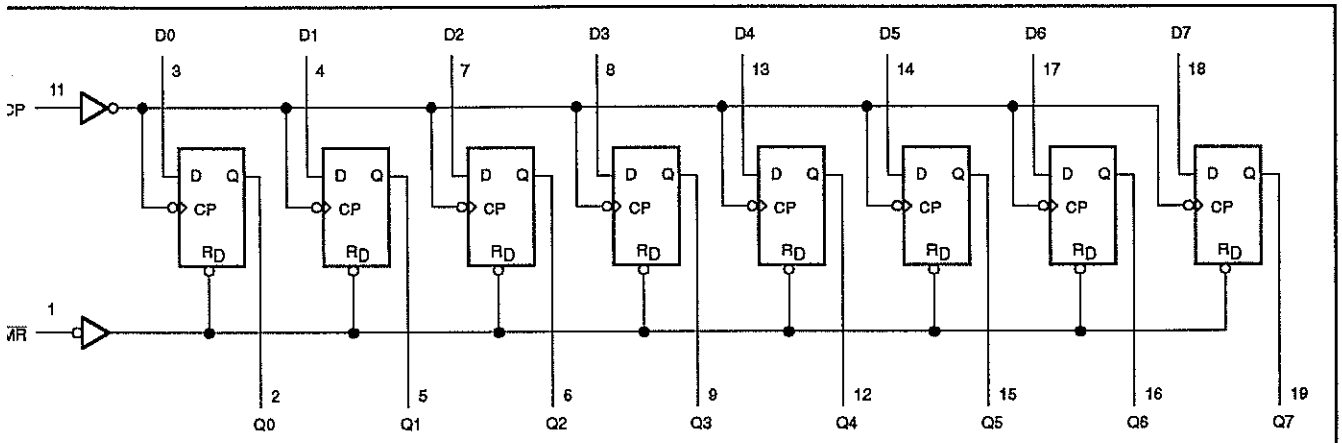
SA00054

LOGIC SYMBOL



SA00053

)GIC DIAGRAM



SA00055

JNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
MR	CP	Dn	Q0 - Q7	
L	X	X	L	Reset (clear)
H	↑	h	H	Load "1"
H	↑	l	L	Load "0"

= High voltage level
= High voltage level one set-up time prior to the Low-to-High clock transition
= Low voltage level
= Low voltage level one set-up time prior to the Low-to-High clock transition
= Don't care
= Low-to-High clock transition

3SOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

)TES:
Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

ECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		-32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

C ELECTRICAL CHARACTERISTICS

YMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V_{RST}	Power-up output low voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or V_I ≤ 4.5V		±5.0	±100		±100	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-70	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		150	250		250	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		24	30		30	mA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One data input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

OTES:
Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
This is the increase in supply current for each input at 3.4V.
For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

C CHARACTERISTICS

ND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40°C to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	250	350		250		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	1	1.5 2.0	3.0 3.4	4.0 4.6	1.5 2.0	4.8 4.8	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn	2	2.5	4.5	6.0	2.5	6.6	ns

C SETUP REQUIREMENTS

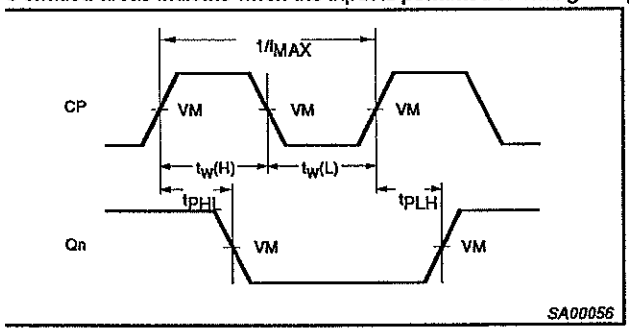
ID = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C V_{CC} = +5.0V		T_{amb} = -40°C to +85°C V_{CC} = +5.0V ±0.5V	
			Min	Typ	Min	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to CP	3	1.5 1.5	0.6 0.4	1.5 1.5	
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CP	3	0.7 0.7	-0.5 -0.5	0.7 0.7	ns
$t_w(H)$ $t_w(L)$	Clock pulse width High or Low	1	1.5 2.0	0.8 1.0	1.5 2.0	ns
$t_w(L)$	Master Reset pulse width, Low	2	1.5	0.8	1.5	ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	1.5	0.5	1.5	ns

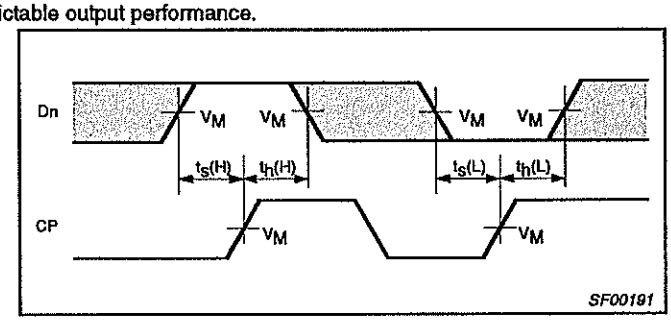
C WAVEFORMS

= 1.5V, V_{IN} = GND to 3.0V

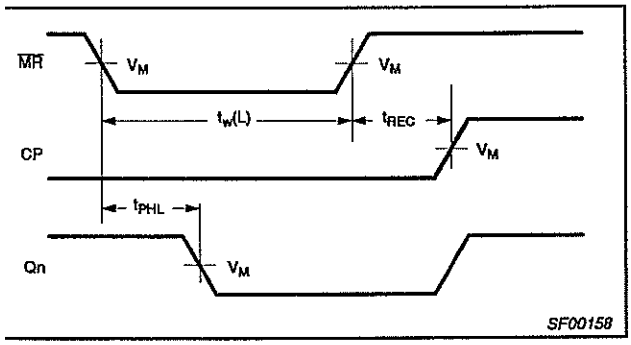
e shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

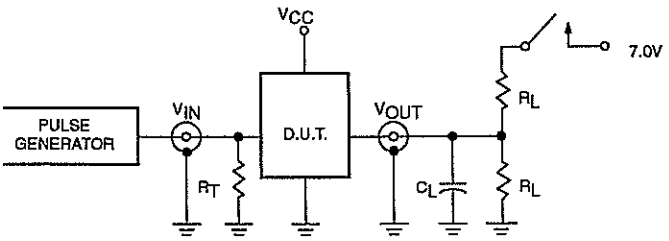


Waveform 3. Data Setup and Hold Times

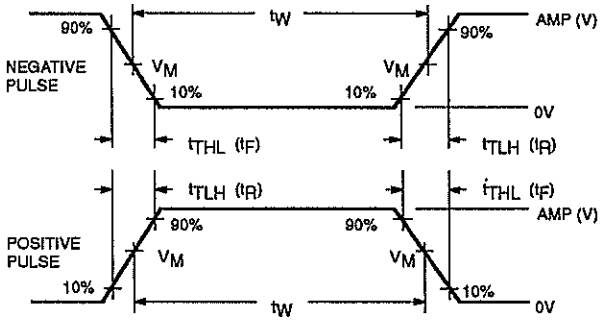


Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

:ST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
All	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00057

Timer — NE/SA/SE555/SE555C

DESCRIPTION

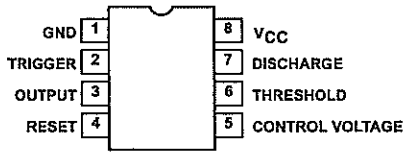
The 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA.

FEATURES

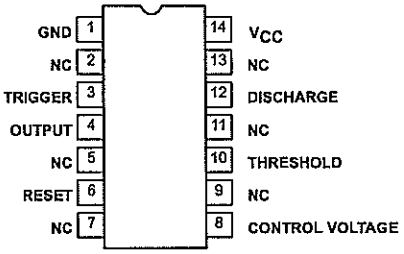
- Turn-off time less than 2µs
- Max. operating frequency greater than 500kHz
- Timing from microseconds to hours
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C

PIN CONFIGURATIONS

D, N, FE Packages



F Package



TOP VIEW

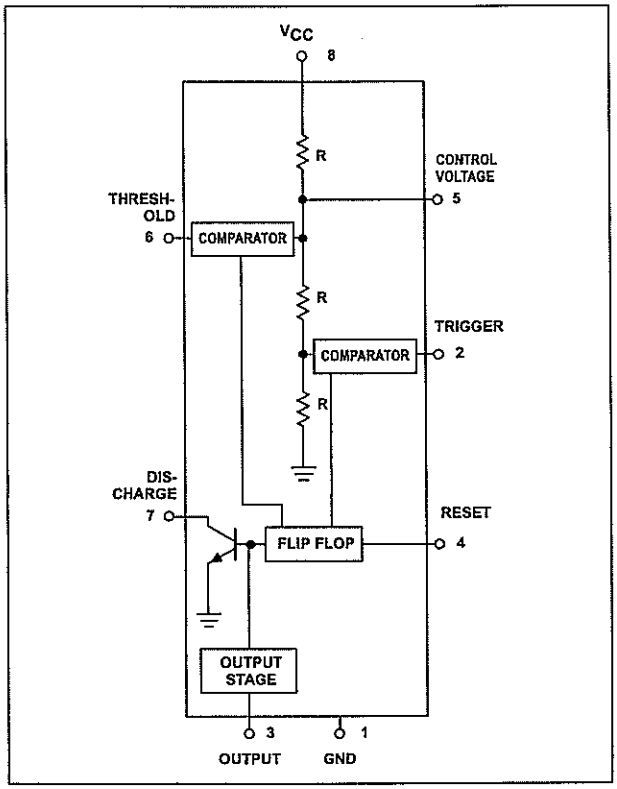
APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation

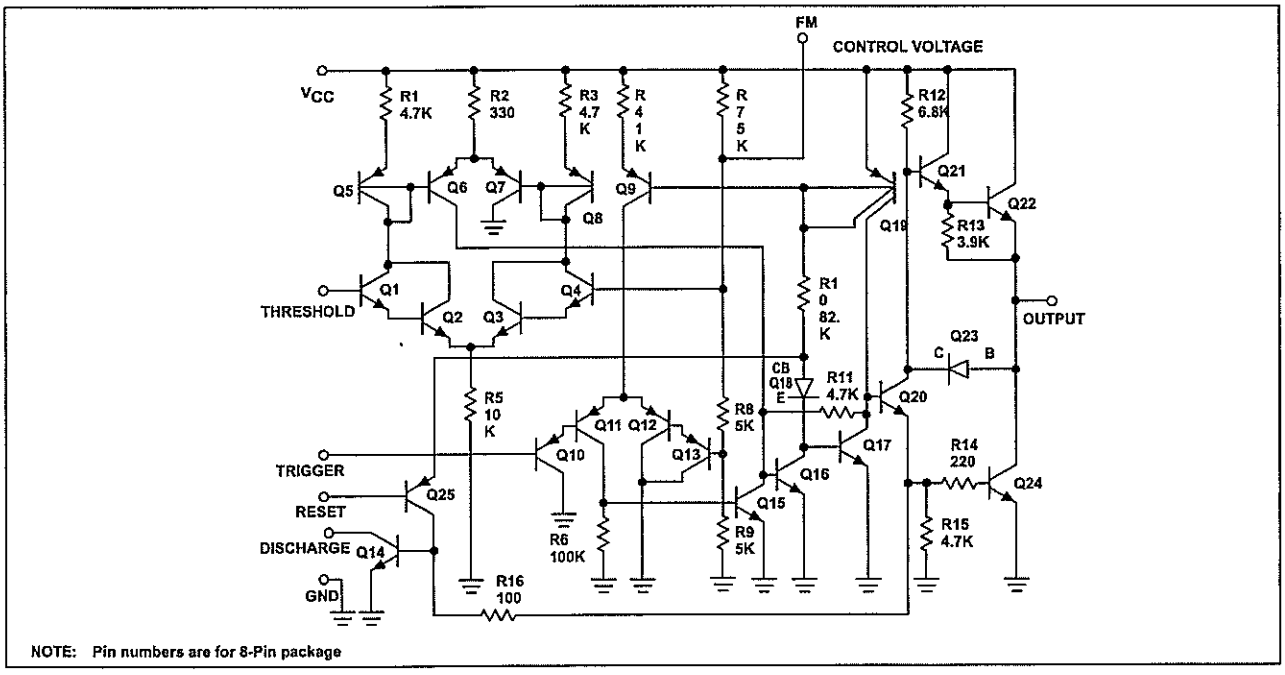
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) Package	0 to +70°C	NE555D	0174C
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE555N	0404B
8-Pin Plastic Dual In-Line Package (DIP)	-40°C to +85°C	SA555N	0404B
8-Pin Plastic Small Outline (SO) Package	-40°C to +85°C	SA555D	0174C
8-Pin Hermetic Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE555CFE	
8-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE555CN	0404B
14-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE555N	0405B
8-Pin Hermetic Cerdip	-55°C to +125°C	SE555FE	
14-Pin Ceramic Dual In-Line Package (CERDIP)	0 to +70°C	NE555F	0581B
14-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE555F	0581B
14-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE555CF	0581B

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



NOTE: Pin numbers are for 8-Pin package

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage		
	SE555	+18	V
	NE555, SE555C, SA555	+16	V
P_D	Maximum allowable power dissipation[1]	600	mW
T_A	Operating ambient temperature range		
	NE555	0 to +70	°C
	SA555	-40 to +85	°C
	SE555, SE555C	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

NOTES:

1. The junction temperature must be kept below 125°C for the D package and below 150°C for the FE, N and F packages. At ambient temperatures above 25°C, where this limit would be derated by the following factors:
   D package 160°C/W
   FE package 150°C/W
   N package 100°C/W
   F package 105°C/W

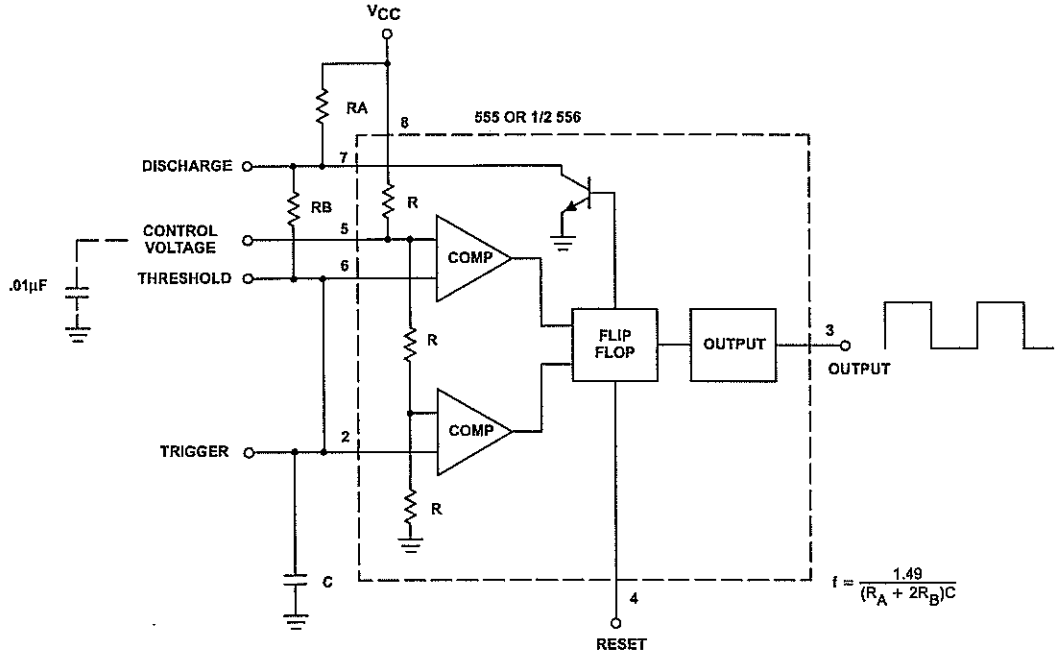
DC AND AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +5V to +15 unless otherwise specified.

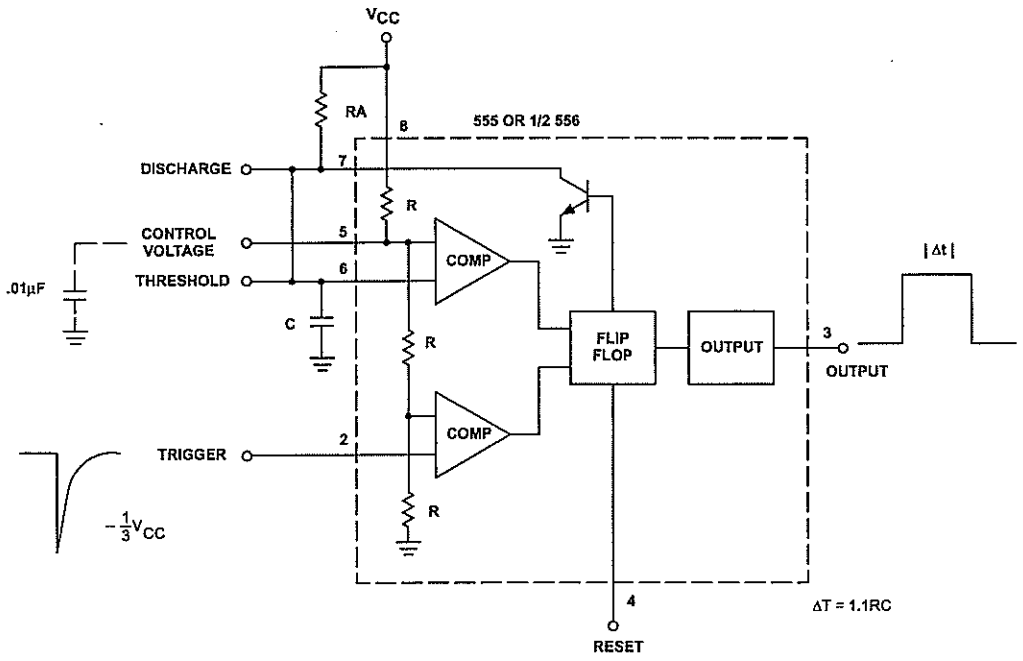
SYMBOL	PARAMETER	TEST CONDITIONS	SE555			NE555/SE555C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		4.5		18	4.5		16	V
I_{CC}	Supply current (low state)[1]	V_{CC}=5V, R_L=∞		3	5		3	6	mA
		V_{CC}=15V, R_L=∞		10	12		10	15	mA
	Timing error (monostable)	R_A=2kΩ to 100kΩ							
t_M	Initial accuracy[2]	C=0.1µF		0.5	2.0		1.0	3.0	%
$\Delta t_M/\Delta T$	Drift with temperature			30	100		50	150	ppm/°C
$\Delta t_M/\Delta V_S$	Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
	Timing error (astable)	R_A, R_B=1kΩ to 100kΩ							
t_A	Initial accuracy[2]	C=0.1µF		4	6		5	13	%
$\Delta t_A/\Delta T$	Drift with temperature	V_{CC}=15V			500			500	ppm/°C
$\Delta t_A/\Delta V_S$	Drift with supply voltage			0.15	0.6		0.3	1	%/V
V_C	Control voltage level	V_{CC}=15V	9.6	10.0	10.4	9.0	10.0	11.0	V
		V_{CC}=5V	2.9	3.33	3.8	2.6	3.33	4.0	V
V_{TH}	Threshold voltage	V_{CC}=15V	9.4	10.0	10.6	8.8	10.0	11.2	V
		V_{CC}=5V	2.7	3.33	4.0	2.4	3.33	4.2	V
I_{TH}	Threshold current[3]			0.1	0.25		0.1	0.25	µA
V_{TRIG}	Trigger voltage	V_{CC}=15V	4.8	5.0	5.2	4.5	5.0	5.6	V
		V_{CC}=5V	1.45	1.67	1.9	1.1	1.67	2.2	V
I_{TRIG}	Trigger current	V_{TRIG}=0V		0.5	0.9		0.5	2.0	µA
V_{RESET}	Reset voltage[4]	V_{CC}=15V, V_{TH} =10.5V	0.3		1.0	0.3		1.0	V
I_{RESET}	Reset current	V_{RESET}=0.4V		0.1	0.4		0.1	0.4	mA
	Reset current	V_{RESET}=0V		0.4	1.0		0.4	1.5	mA
V_{OL}	Output voltage (low)	V_{CC}=15V							
		I_{SINK}=10mA		0.1	0.15		0.1	0.25	V
		I_{SINK}=50mA		0.4	0.5		0.4	0.75	V
		I_{SINK}=100mA		2.0	2.2		2.0	2.5	V
		I_{SINK}=200mA		2.5			2.5		V
		V_{CC}=5V							
		I_{SINK}=8mA		0.1	0.25		0.3	0.4	V
		I_{SINK}=5mA		0.05	0.2		0.25	0.35	V
V_{OH}	Output voltage (high)	V_{CC}=15V							
		I_{SOURCE}=200mA		12.5			12.5		V
		I_{SOURCE}=100mA	13.0	13.3		12.75	13.3		V
		V_{CC}=5V							
		I_{SOURCE}=100mA	3.0	3.3		2.75	3.3		V
t_{OFF}	Turn-off time[5]	V_{RESET}=V_{CC}		0.5	2.0		0.5	2.0	µs
t_R	Rise time of output			100	200		100	300	ns
t_F	Fall time of output			100	200		100	300	ns
	Discharge leakage current			20	100		20	100	nA

NOTES:
1. Supply current when output high typically 1mA less.
2. Tested at V_{CC}=5V and V_{CC}=15V.
3. This will determine the max value of R_A+R_B, for 15V operation, the max total R=10MΩ, and for 5V operation, the max. total R=3.4MΩ.
4. Specified with trigger input high.
5. Time measured from a positive going input pulse from 0 to 0.8xV_{CC} into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

TYPICAL APPLICATIONS



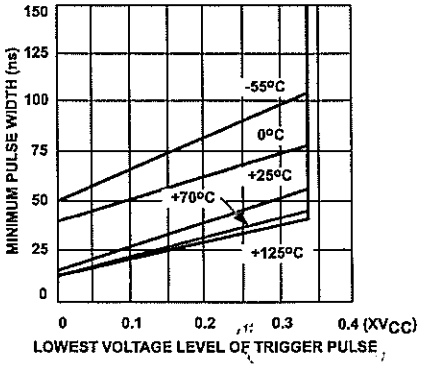
Astable Operation



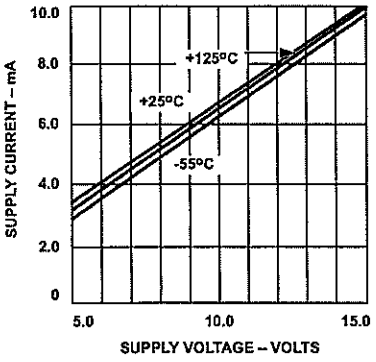
Monostable Operation

TYPICAL PERFORMANCE CHARACTERISTICS

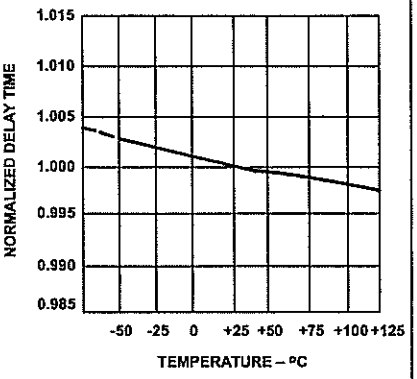
Minimum Pulse Width Required for Triggering



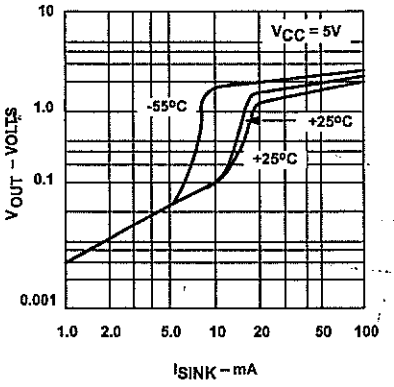
Supply Current vs Supply Voltage



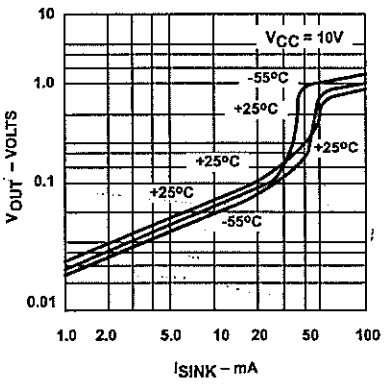
Delay Time vs Temperature



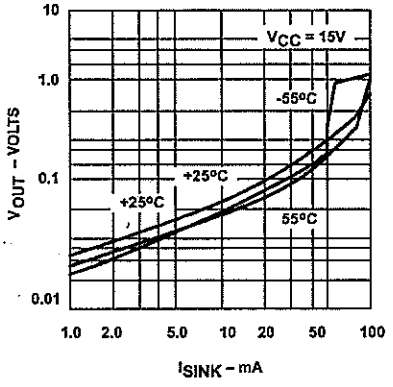
Low Output Voltage vs Output Sink Current



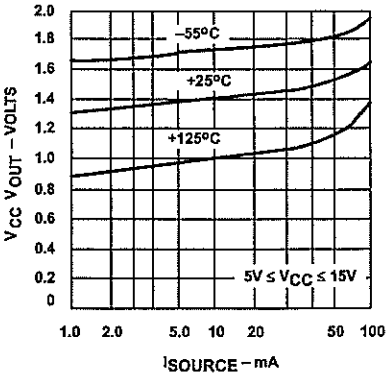
Low Output Voltage vs Output Sink Current



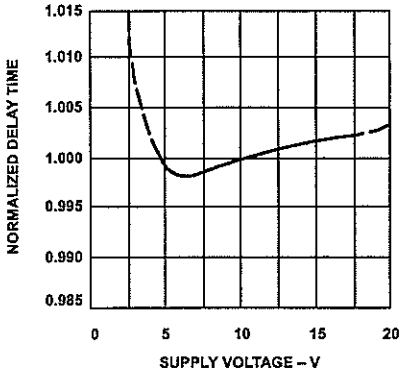
Low Output Voltage vs Output Sink Current



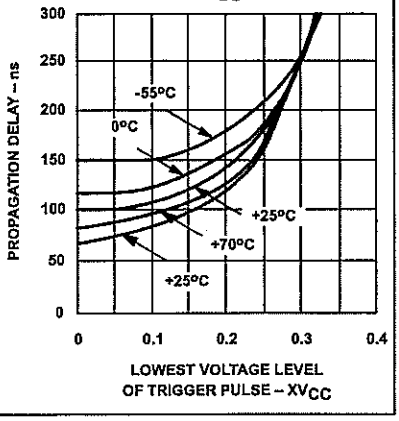
High Output Voltage Drop vs Output Source Current



Delay Time vs Supply Voltage



Propagation Delay vs Voltage Level of Trigger Pulse



TYPICAL APPLICATIONS

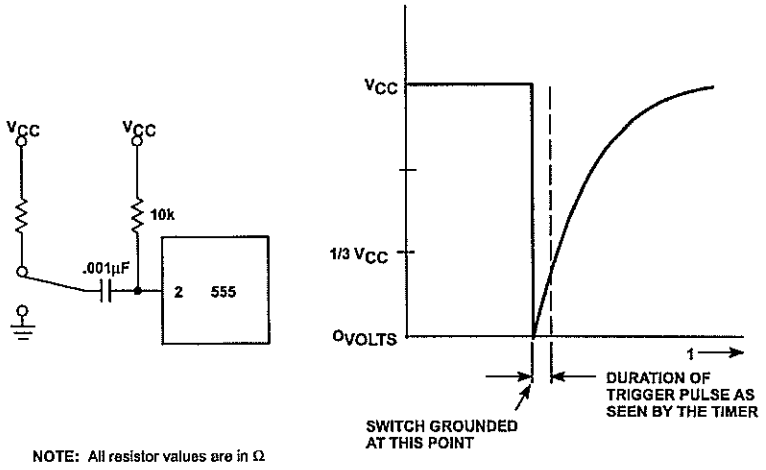


Figure 1. AC Coupling of the Trigger Pulse

Trigger Pulse Width Requirements and Time Delays

Due to the nature of the trigger circuitry, the timer will trigger on the negative going edge of the input pulse. For the device to time out properly, it is necessary that the trigger voltage level be returned to some voltage greater than one third of the supply before the time out period. This can be achieved by making either the trigger pulse sufficiently short or by AC coupling into the trigger. By AC coupling the trigger, see Figure 1, a short negative going pulse is achieved when the trigger signal goes to ground. AC coupling is most frequently used in conjunction with a switch or a signal that goes to ground which initiates the timing cycle. Should the trigger be held low, without AC coupling, for a longer duration than the timing cycle the output will remain in a high state for the duration of the low trigger signal, without regard to the threshold comparator state. This is due to the predominance of Q_{15} on the base of Q_{16}, controlling the state of the bi-stable flip-flop. When the trigger signal then returns to a high level, the output will fall immediately. Thus, the output signal will follow the trigger signal in this case.

Another consideration is the "turn-off time". This is the measurement of the amount of time required after the threshold reaches 2/3 V_{CC} to turn the output low. To explain further, Q_1 at the threshold input turns on after reaching 2/3 V_{CC}, which then turns on Q_5, which turns on Q_6. Current from Q_6 turns on Q_{16} which turns Q_{17} off. This allows current from Q_{19} to turn on Q_{20} and Q_{24} to given an output low. These steps cause the 2µs max. delay as stated in the data sheet.

Also, a delay comparable to the turn-off time is the trigger release time. When the trigger is low, Q_{10} is on and turns on Q_{11} which turns on Q_{15}. Q_{15} turns off Q_{16} and allows Q_{17} to turn on. This turns off current to Q_{20} and Q_{24}, which results in output high. When the trigger is released, Q_{10} and Q_{11} shut off, Q_{15} turns off, Q_{16} turns on and the circuit then follows the same path and time delay explained as "turn off time". This trigger release time is very important in designing the trigger pulse width so as not to interfere with the output signal as explained previously.

. Tijdbasisschakelingen.

ds enkele jaren worden er tijdbasisschakelingen ontwikkeld, die met een minimum aan uitwendige nponenten zich lenen tot de samenstelling van astabiele- en monostabiele multivibratoren, van Schmitt-igers, enz,...

n populair en veel gebruikt IC is de 555. Deze IC kan doelmatig werken met een voedingsspanning sen *4,5* en *16 V*, en schakelt stromen tot *200* mA, terwijl hij praktisch ongevoelig is voor temperatuur-ommelingen. Hij is compatibel met elke IC-familie. De IC is verpakt in een 8-pens DIL behuizing.

IC 556 is een gelijkaardig IC die tweemaal de schakeling van de 555 bevat in één behuizing.

1 Opbouw en werking.

In figuur 5.1 wordt het blokschema van de 555 voorgesteld. De schakeling is opgebouwd rond twee comparatoren waarvan de uitgangen een SR-flipflop sturen. Op de uitgang van de flipflop is een ontlaadtransistor geschakeld. De FF stuurt ook een eindtrap, en een resistief netwerk.

- Als de triggerspanning (klem 2) kleiner wordt dan *1/3* U_B zal de uitgang van de OPAMP 2 naar een hoog niveau schakelen. Hierdoor wordt de SR-flipflop geset. *(Q = 1).*

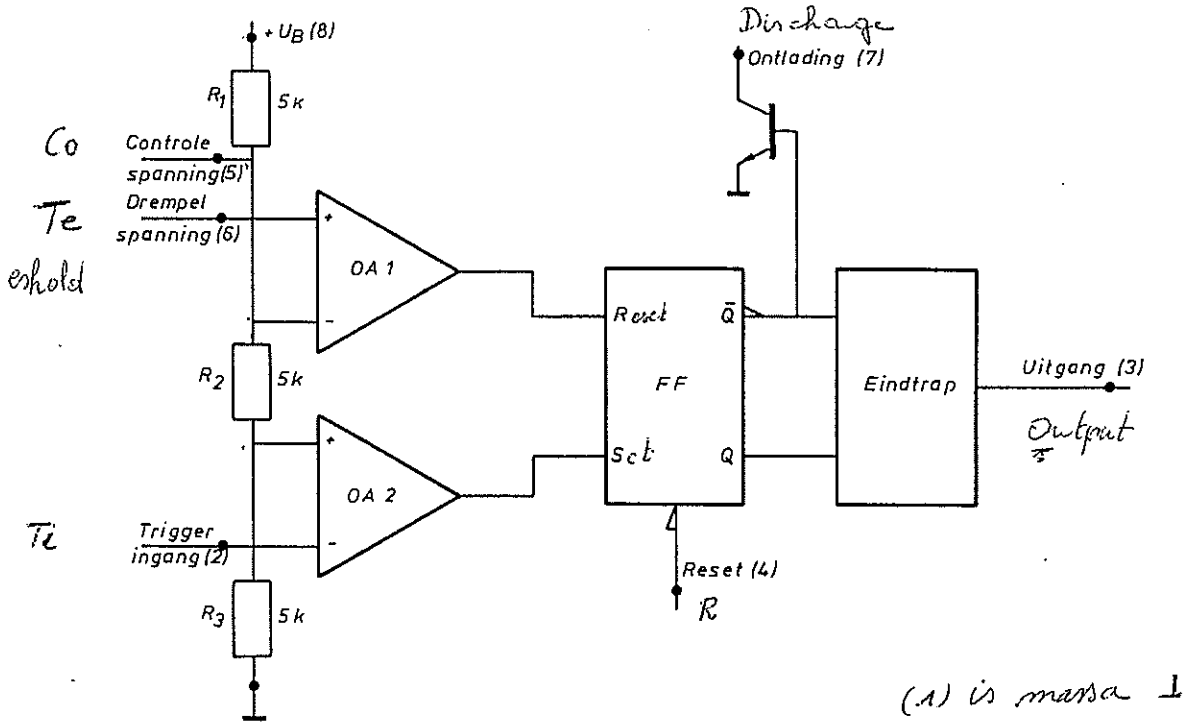


Fig. 5.1. Blokschema van de 555

Door de geheugenwerking van de flipflop blijft deze toestand behouden als de triggerspanning wegvalt. Het lage niveau aan de complementaire uitgang $\bar{Q}$ brengt de ontlaadtransistor in gesperde toestand.

- Als de drempelspanning (klem 6) groter wordt dan *2/3* U_B zal de uitgang van OPAMP 1 naar een hoog niveau schakelen. De flipflop wordt hierdoor gereset *(Q = 0).* Uiteraard blijft deze toestand ook behouden bij het wegvallen van de drempelspanning. Het hoog niveau van $\bar{Q}$ maakt de ontlaadtransistor geleidend.
- Een aktief laag signaal op de reset-ingang brengt de uitgang van de IC op een laag niveau. Door de prioriteit van dit signaal ten opzichte van de andere ingangssignalen, kan de werking van de schakeling gedurende welbepaalde tijdsintervallen onderbroken worden.

De werking van de 555 kunnen we als volgt samenvatten:

- De uitgang kan hoog gemaakt worden door een triggersignaal dat lager is dan *1/3* U_B.
- Deze toestand blijft behouden tot de drempelspanning groter wordt dan *2/3* U_B.
- Door toepassing van een controlespanning (op klem 5) is het mogelijk willekeurige spanningsniveaus in te stellen.

Logboek

Logboek: Jonas Anrijs

datum	*onderwerp*	*tijd*
11/09/00	Bibliotheek zoeken	0u30
13/09/00	Opstellen inhoudstafel	1u30
04/11/00	Samenkomen	6u30
27/12/00	Samenkomen	6u00
02/02/00	Bibliotheek zoeken	5u00
20/02/00	Tekening maken	4u00
24/02/00	Bezoek radartoren	3u00
15/03/00	Samenkomen	1u30
1!/03/00	Tekening maken	1u00
20/03/00	Verkeersradar	2u00
25/03/00	Internetten	3u00
26/03/00	SAR	2u00
01/04/00	SAR	3u00
02/04/00	SAR	3u00
06/04/00	proefpresentatie	5u30
07/04/00	proefpresentatie	3u20
26/04/00	SAR	4u00
11/05/00	Labometingen	5u30
13/05/00	Afwerken moderne toepassingen	2u00
17/05/00	Verslag bezoek radar in Zeebrugge	2u30
18/05/00	Labometingen	3u00
19/05/00	Samenkomen	5u00
23/05/00	Afwerking en lay-out	5u00
24/05/00	Afwerking en lay-out	9u00

Logboek: Tom Derous

datum	*onderwerp*	*tijd*
13/09/99	Opstellen voorlopige inhoudstafel	1h30
03/10/99	Informatie opzoeken: principiële werking	1h30
04/10/99	Uitwerken grondbegrippen	1h00
11/10/99	Informatie zoeken: internet	2h00
04/11/99	Samen werken aan GIP	6h30
26/12/99	Ingeleverd stuk verbeteren	0h30
27/12/99	Samen werken aan GIP	1h30
07/02/00	Informatie zoeken: golven en trillingen	3h00
19/02/00	Beginnen uitwerken golven en trillingen	2h00
24/02/00	Bezoek radartoren	3u00
14/03/00	Golven en trillingen	1h30
15/03/00	Bespreken 'wat nog te doen'	1h00
06/04/00	Voorbereiden voorstelling	3h00
10/04/00	Figuren tekenen voor golven en trillingen	1h00
06/05/00	Uitwerken ultrasone golven en microgolven	3h00
07/05/00	Uitwerken reflectie, diffractie en refractie	1h30
10/05/00	Informatie zoeken: klystron + uitwerken	1h30
14/05/00	Uitwerken bundelen van geluidsgolven	0h30
15/05/00	Bijwerken en verbeteren golven	2h30
16/05/00	Verder uitwerken klystron	1h00
17/05/00	Afwerken hoofdstuk	1h30
18/05/00	Onderverdeling + inhoudstabel maken	0h30
19/05/00	Stukken samenbrengen + veranderen inhoudstafel	4h00
20/05/00	Maken van het logboek	1h00
21/05/00	Figuren nummeren + spellingscontrole	2h30
22/05/00	Alles in het juiste opmaakprofiel + controle	1h30
23/05/00	Uitwerken transducer + alles in orde doen	5h45

Logboek: Jonas Missiaen

datum	*onderwerp*	*tijd*
01/09/99	Zoeken op internet	1u00
08/09/99	Bibliotheek KHBO Oostende	4u00
12/09/99	Lezen boeken	2u00
13/09/99	Opstellen inhoudstafel	1u30
18/09/99	Tekenen	0u45
20/09/99	Tekst + tekeningen analoge verwerking	1u00
22/09/99	Vervolg	2u00
30/09/99	Verbeteren tekening + tekst	0u20
06/10/99	Vervolg	1u00
24/10/99	Lezen	1u30
02/11/99	Verbeteren tekst	1u30
04/11/99	Samenkomen	6u30
27/12/99	Samenkomen	6u00
30/12/99	Ontwerpen schakeling	1u20
04/01/00	Vervolg	1u00
06/01/00	Vervolg	0u30
12/01/00	Vervolg	2u00
16/01/00	Vervolg	1u30
19/01/00	Vervolg	2u00
22/01/00	Tekst	3u00
23/01/00	Tekst + tekeningen	3u00
25/01/00	Vervolg	1u00
26/01/00	Vervolg	2u00
29/01/00	Vervolg	1u30
31/01/00	Vervolg	1u20
06/02/00	Vervolg	2u30
08/02/00	Zoeken op internet	0u40
09/02/00	Engelse tekst zoeken	1u20
14/02/00	Bezoek aan de verkeerstoren van Zeebrugge	3u00
17/02/00	Verbeteren tekst	2u00
19/02/00	Verbeterentekst + aanmaken opmaakprofielen	5u30
20/02/00	Vervolg	0u30
08/03/00	Ontwerpen schakeling + tekst en tekeningen	4u00
09/03/00	Vervolg tekst	1u30
15/03/00	Samenkomen	1u30
18/03/00	Presentatie maken	2u00
22/03/00	Vervolg	0u30
25/03/00	Vervolg	0u30
06/04/00	Presentatie afwerken	5u30
07/04/00	Proefpresentatie	3u20
22/04/00	Tekst digitale sinus	3u00
23/04/00	Vervolg + snelheidsbepaling	3u30
24/04/00	Snelheidsbepaling	4u00
26/04/00	Hoekbepaling	2u00
29/04/00	Vervolg	3u30
30/04/00	Vervolg + voorbereiding labometingen +opzoeken in data bladen	2u40

01/05/00	Vervolg	4u00
02/05/00	Vervolg	2u30
03/05/00	Vervolg	3u00
04/05/00	Vervolg	1u20
06/05/00	Vervolg + vervolg hoekmeting	5u30
07/05/00	Vervolg snelheidsbepaling	3u40
08/05/00	Vervolg	2u00
09/05/00	Opzoeken in databoeken	1u30
10/05/00	Solderen schakeling	4u20
13/05/00	Verbeteren tekst	2u30
14/05/00	Voorbereiding opendeurdag	3u15
15/05/00	Opzoeken in databoeken	1u20
17/05/00	Solderen	3u20
18/05/00	Metingen	3u00
19/05/00	Samenkomen opmaak	5u00
23/05/00	Afwerking en lay-out	5u30

Logboek: Gerd Vermont

datum	*onderwerp*	*tijd*
08/09/00	Boeken gezocht in KHBO Oostende	4u00
13/09/99	Opstellen inhoudstafel	1u30
22/09/99	Opstellen impulslengte, doppler-effect	1u00
02/10/99	Samenvatten boek golven (hfst1)	1u00
03/10/99	Idem + zoeken info opwekken golven, wetten maxwell,...	
09/10/99	Lezen GIP: elektromagn. Golven (David d'Hondt)	2u30
	Bib: boeken verlengen	
	Lezen: eindwerk 'US-radarsysteem'	
14/10/99	Kopiëren uit boek: RADAR: theorie en praktijk	0u30
16/10/99	Terugbrengen boeken KHBO	2u00
03/11/99	Zoeken informatie BIB. Brugge	1u00
04/11/99	Afwerken 1^{e} versie (Bij Tom Derous)	6u30
25/12/99	Lezen boeken elektronica	1u00
26/12/99	Lezen boeken elektronica	1u00
27/12/99	Samenkomen	6u00
28/12/99	Bibliotheek	2u00
29/12/99	Lezen cursus elektronica: de transistor	1u00
24/02/00	Bezoek radartoren	3u00
04/03/00	Polarisatiemethodes (algemeen)	2u00
06/03/00	Idem + aanbrengen verbeteringen	3u00
07/03/00	Stabiliteisfactoren (met Rb aan collector)	4u00
09/03/00	Stabiliteitsfactor (met spanningsdeler)	4u00
10/03/00	Bekijken signaalvervangsschema's + stabiliteitsfactoren	3u00
11/03/00	Bekijken signaalvervangsschema's	4u00
15/03/00	Samenkomen: afspraken i.v.m. proefpresentatie	1u30
06/04/00	Voorbereiding proefpresentatie	5u30
07/04/00	Voorbereiding proefpresentatie + presentatie	3u20
11/04/00	Signaalvervangschema 's uitwerken	2u20
13/04/00	Signaalvervangschema 's uitwerken	2u00
15/04/00	Oscillatoren	2u00
	Bib: boeken gezocht	
17/04/00	Proberen inzicht te krijgen in oscillatoren	2u00
18/04/00	Katalogus gekocht in elektro 8000 + info US luidspr. Gevraagd	3u00
	Praktisch ontwerp: 2-traps versterker (werkt)	
19/04/00	Praktisch ontwerp: 3-traps versterker (werkt)	5u00
	Opstellen formules oscillatoren (Colpitts-Hartley en Clopp osc.)	
	Logboek typen	
20/04/00	Proberen opstellen formules oscillator met afg. Collecorketen	1u00
22/04/00	Aanbrengen verbeteringen	2u00
	Labometing II, III en IIII opstellen	
23/04/00	Lezen: LF – vermogenversterkers	2u00
24/04/00	Opstellen inleiding hoofdstuk 4	3u00
	Aanbrengen verbeteringen	
06/05/00	Versterker met tegenkoppeling, versterker in GCS	4u00
07/05/00	Voorgaande berekeningen	4u00
09/05/00	Intikken + verbeteren voorgaande berekeningen	4u00

10/05/00	Solderen versterker I + componenten gaan halen	4u00
11/05/00	Labometing op versterker I	5u30
12/05/00	Verwerking meetresultaten	2u00
17/05/00	Solderen versterker I + intikken bijgewerkt ontwerp	4u00
18/05/00	Labometing op versterker I	3u00
19/05/00	Samenkomen Layout	5u00
20/05/00	Verwerking meetresultaten	7u00
	Layout hoofdstuk 4 bijwerken	
	Oscillator met afgestemde collectorketen	
	Layout hoofdstuk 2 bijwerken	
21/05/00	Bijwerken layout hoofdstuk 4	2u00
22/05/00	Inscannen bijlagen + foto's zeebrugge	7u00
	Verbeteringen aanbrengen (hfst.4)	
	Hoofdstukken 2,3 en 4 samenbrengen + layout	
23/05/00	Afwerking en lay-out	8u00
24/05/00	Afwerking en lay-out	9u00